SYSTEM SCHEMATICS

A2060/A2065/A2232

AUGUST, 1990 PN-314042-01

Commodore

Produced By:

Commodore International Spare Parts GmbH
Braunschweig, West Germany

SYSTEM SCHEMATICS

A2060/A2065/A2232

AUGUST, 1990 **PN-314042-01**

INTERNATIONAL EDITION

COMMODORE "INTERNATIONAL EDITION" SERVICE MANUALS CONTAIN PART NUMBER INFORMATION WHICH MAY VARY ACCORDING TO COUNTRY. SOME PARTS MAY NOT BE AVAILABLE IN ALL COUNTRIES.

Commodore Business Machines, Inc.
1200 Wilson Drive, West Chester, Pennsylvania 19380 U.S.A.

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A2060 — ARCNET CONTROLLER FOR A2000

DIMENSIONS:	13.25 x 4.5 inches
WEIGHT:	1 lb.
ENVIRONMENTAL:	0C to 70C Operating
POWER REQUIREMENTS:	+5V @ 1.75A max −5V @ 0.27A max
INCLUDES:	• A2060 PCB • BNC "T" connector • BNC to BNC cable (2 meter) • 93 ohm network terminator
FEATURES:	• Support of ArcNet bus protocol (uses HIT module) • Socket for optional network Autoboot ROM • Novelle netware software optionally available
ARCNET HAS THE FOLLOWING FEATURES:	• Allows up to 256 nodes • Maximum distance of 2000 feet between nodes • Data rate of 2.5 Mbps

GENERAL DESCRIPTION

The A2060 is an ARCNET controller designed for use with the A2000 computer. ARCNET is a local area network utilizing a self-polling "modified token passing" scheme operating at a 2.5 Mbit data rate. A "modified token passing" scheme is one in which all token passes are acknowledged by the node accepting the token. The token passing network avoids the fluctuating channel access times caused by data collisions in so-called CSMA/CD schemes such as Ethernet.

The A2060 plugs into one of the 100 pin expansion slots in the A2000. The BNC plug on the rear of the A2060 connects to the network in daisy chain fashion with the special "T" connector and BNC to BNC cable included. Note that most network installations will require additional cabling and active links, and that network software is not included.

ENVIRONMENTAL TEST REQUIREMENTS

Units shall comply with the following environmental resistance requirements.

TEMPERATURE	
Operational	5 to 55°C
Storage	−20 to +70°C
Gradient	+10°C/hour
Temperature Cycle	−20 to 60° C, 10 cycles, 10 minutes minimum at each extreme, 5 minutes maximum between extremes
HUMIDITY	
Operational (relative)	10 to 90% (non-condensing)
Storage (relative)	5 to 95% (non-condensing)
VIBRATION	
Non-operating (randomfrequency)	5.2 Gs per MIL-STD 202 Method 214, 15 min. in each of three axes
SHOCK	
Operational	5 Gs to each of 6 axes, two 11 mSec half sinewave shocks
Non-Operational	20 Gs applied as above
ALTITUDE	
Operational	0 to 3000 meters
Non-Operational	0 to 15,000 meters

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Commodore International Spare Parts List
SHIPPING ASSEMBLIES

Commodore part numbers are provided for reference only and do not indicate the availability of spare parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Part number information may vary according to country, some parts may not be available in all countries.

532060-01	A2060 SHIPPING ASSY (U.S.)
363035-05	BOX BULK PACKING
363097-05	BOX PACKING
318928-01	BAG PLASTIC CONDUCTIVE
363350-01	MANUAL USER A2060 (EFIGS)
318290-01	CARD WARRANTY U.S.
314877-04	SERVICE CENTER LIST (U.S.)
316846-01	LABEL UPC A2060
390627-01	CONNECTOR BNC "T"
390628-01	TERMINATOR BNC 93 OHMS
312839-01	CABLE BNC 2 M LG.
311661-01	PCB ASSY A2060, REV. 2
251006-01	BAG PLASTIC

532060-02	A2060 SHIPPING ASSY (CANADA)
363035-05	BOX BULK PACKING
363097-05	BOX PACKING
318928-01	BAG PLASTIC CONDUCTIVE
363350-01	MANUAL USER A2060 (EFIGS)
318882-01	CARD WARRANTY CANADA
316846-01	LABEL UPC A2060
390627-01	CONNECTOR BNC "T"
390628-01	TERMINATOR BNC 93 OHMS
312839-01	CABLE BNC 2 M LG.
311661-01	PCB ASSY A2060, REV. 2
251006-01	BAG PLASTIC

532060-03	A2060 SHIPPING ASSY (AUSTRALIA)
363035-05	BOX BULK PACKING
363097-05	BOX PACKING
318928-01	BAG PLASTIC CONDUCTIVE
363350-01	MANUAL USER A2060 (EFIGS)
318884-01	CARD WARRANTY AUSTRALIA
316846-01	LABEL UPC A2060
390627-01	CONNECTOR BNC "T"
390628-01	TERMINATOR BNC 93 OHMS
312839-01	CABLE BNC 2 M LG.
311661-01	PCB ASSY A2060, REV. 2
251006-01	BAG PLASTIC

532060-04	A2060 SHIPPING ASSY (GERMANY)
363035-05	BOX BULK PACKING
363097-05	BOX PACKING
318928-01	BAG PLASTIC CONDUCTIVE
363350-01	MANUAL USER A2060 (EFIGS)
316846-01	LABEL UPC A2060
390627-01	CONNECTOR BNC "T"
390628-01	TERMINATOR BNC 93 OHMS
312839-01	CABLE BNC 2 M LG.
311661-01	PCB ASSY A2060, REV. 2
251006-01	BAG PLASTIC

532060-05	A2060 SHIPPING ASSY (EUROPE)
363035-05	BOX BULK PACKING
363097-05	BOX PACKING
318928-01	BAG PLASTIC CONDUCTIVE
363350-01	MANUAL USER A2060 (EFIGS)
316846-01	LABEL UPC A2060
390627-01	CONNECTOR BNC "T"
390628-01	TERMINATOR BNC 93 OHMS
312839-01	CABLE BNC 2 M LG.
311661-01	PCB ASSY A2060, REV. 2
251006-01	BAG PLASTIC

532060-06	A2060 SHIPPING ASSY (SCANDINAVIAN)
363035-05	BOX BULK PACKING
363097-05	BOX PACKING
318928-01	BAG PLASTIC CONDUCTIVE
363351-01	MANUAL USER A2060 (SCAND)
316846-01	LABEL UPC A2060
390627-01	CONNECTOR BNC "T"
390628-01	TERMINATOR BNC 93 OHMS
312839-01	CABLE BNC 2 M LG.
311661-01	PCB ASSY A2060, REV. 2
251006-01	BAG PLASTIC

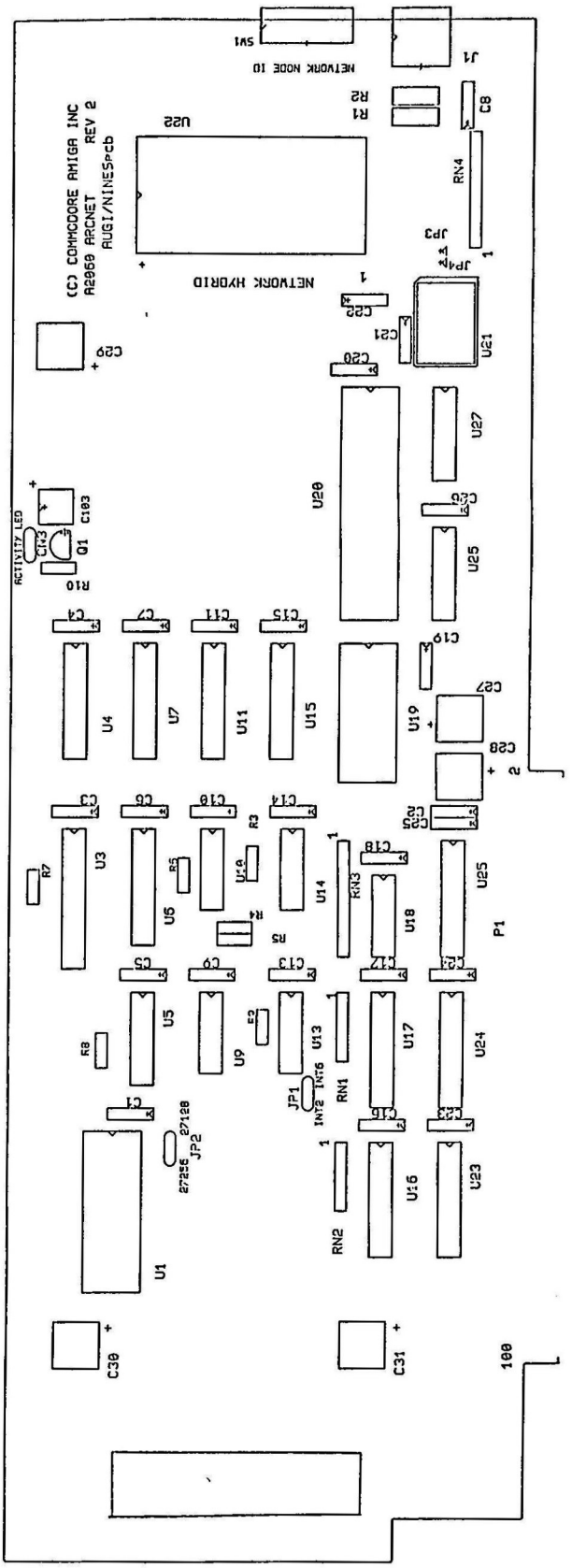
4 2 2 3 2

Commodore International Spare Parts List
PCB Components
PCB Assembly #311611-01

Commodore part numbers are provided for reference only and do not indicate the availability of spare parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Part number information may vary according to country, some parts may not be available in all countries.

IC COMPONENTS		
390554-01	16L8A PAL CONTROL 1	U6
390553-01	20L10A PAL CONTROL 2	U3
390585-01	27C64-20 EPROM	U1
901521-13	74LS244	U4,U7,U24,U25
901521-29	74LS373	U11,U15
901521-31	74LS32	U18
901521-34	74LS175	U5
901521-46	74LS245	U23
901521-71	74LS166	U26
318041-01	74F521	U17
390081-01	74F74	U9,U10
390198-01	74F86	U14
390586-01	74F38	U13
390575-01	LSI LAN COM90C26	U20
390576-01	LSI LAN TRANSCEIVER COM92C3	U27
390577-01	HYB9068 HIT HYBRID MODULE	U22
251637-03	MEM SRAM 2K X 8 BIT 120NS	U19
901521-43	74LS374	U16
325566-21	OSCILLATOR 20MHZ 50MA	U21
SOCKETS		
390060-01	DIP 24 PIN .3"	U3
904150-02	IC L/P 16 PIN .3"	U27
904150-04	IC L/P 24 PIN .6"	U19
904150-05	IC L/P 28 PIN .6"	U1
904150-06	IC L/P 40 PIN .6"	U20
904150-08	IC L/P 20 PIN .3"	U6

RESISTOR NETWORKS		
902441-22	SIP 1K 6 PIN 2%	RN1,RN2
902410-10	SIP 1K 10 PIN	RN3
902410-07	SIP 10K 10 PIN	RN4
RESISTORS		
901550-105	CF 33 OHM 1/4W 5%	R3-R9
901600-51	CF 5.6K 1/2W 5%	R1,R2
901550-49	100 OHM 1/4W 5%	R10
900101-51	2.2 UF ELEC RAD	C103
CAPACITORS		
390082-04	CERM RAD .33UF 50 V	C1-C26
900101-17	ELEC AXL 22 UF 35 V	C28-C31
390101-09	2.2UF ELEC, RAD	C103
CONNECTOR		
390673-01	CONNECTOR INSULATED BNC	J1
MISCELLANEOUS		
390363-02	SWITCH 8 POSITION DIP R/A	SW1
311665-01	OPTION CARD BRACKET	
906800-07	SCREW M3 X .5 X 4 (QTY 2) FOR OPTION CARD BRACKET	
902707-01	TRANSISTOR 2N3906	Q1
903326-03	HEADER, 3 PIN SIL	CN3
316893-01	LABEL, FCC ID	



PCB BOARD LAYOUT #311661, REV. 2

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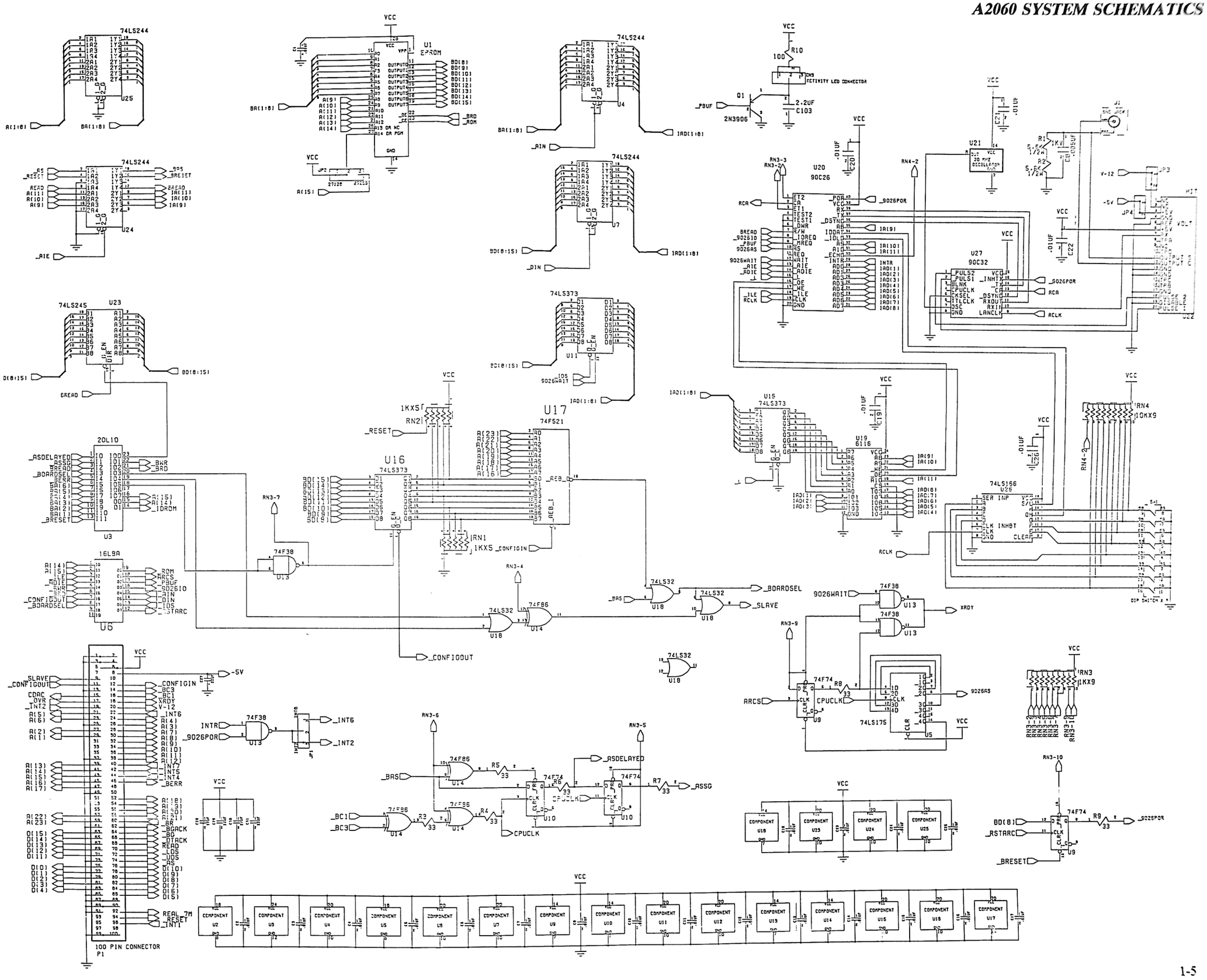
74LS244
U25
74LS244
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74LS245
U23
20L10
U3
16L8A
U6
74LS244
U4
74LS244
U7
74LS373
U11
U1
EPROM
VCC
U17
74F521
U16
74LS373
RN2
1KX5
RESET
RN1
1KX5
CONFIGIN
74F38
U13
74LS32
U18
74F86
U14
74F74
U10
U15
74LS373
U19
6116
U20
90C26
U27
90C32
U21
30 MHZ OSCILLATOR
U26
74LS166
74LS175
U5
U9
R10
100
ACTIVITY LED CONNECTOR
Q1
2N3906
C103
2.2UF
.01UF
R1
1KX1
5.6K 1/2W
R2
5.6K 1/2W
J1
BNC JACK
V-12
-5V
JP3
JP4
RN3-3
RN4-2
RN3-4
RN3-7
RN3-6
RN3-5
RN3-9
RN3-10
RN4
10KX9
RN3
1KX9
100 PIN CONNECTOR
P1
DIP SWITCH X
COMPONENT

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... complete technical discussion

A2232

A2065 FUNCTIONAL SPECIFICATION

DESCRIPTION

The A2065 Ethernet LAN Card controller implements the 802.3 type protocol which calls for a 10 Megabit/sec CSMA/CD interface. It supports both 10Base2 Type B (Cheapernet) and 10 Base5 Type A (thick Ethernet) connections. The design has been developed around the AMD LANCE chipset which is comprised of the Am7990 Local Area Network Controller for Ethernet, the Am7992B Serial Interface Adapter, the Am7996 IEEE-802.3 Ethernet/Cheapernet Transceiver, and other associated logic necessary to implement a complete Ethernet interface.

ARCHITECTURE

A shared memory host interface was chosen because of the bus bandwidth requirements of the Am7990. A total of 32K of onboard buffering is provided to act as a shared interface between the Am7990 and Amiga CPU. This allows for worst case conditions of back to back Ethernet packets received by the board during loaded 68000 or graphics chip activity. In addition to the 32K of memory mapped packet memory, the Am7990's I/O registers are also mapped into the Amiga memory space as two sixteen bit locations. Finally, a small 256*4 Bit Prom is used to store the autoconfig data as well as the board's Ethernet address. The output side consists of both thick and thin (Cheapernet) Ethernet interfaces. The thick interface comes directly from the Am7992B SIA with transformer isolation. To implement the Cheapernet section, various passive components along with an Am7996 are required.

Functionally, the Ethernet interface may be partitioned into the following sections: Transceiver interface, autoconfig and configuration logic, Bus control buffers and logic, and onboard control logic/buffering including the packet memory. In the following sections each subsystem will be explored and discussed in more detail (refer to Figure 1).

TRANSCEIVER INTERFACE

The A2065 supports two types of cable media. The first type is commonly called "Thick Ethernet" or 10Base5. Thick Ethernet is used mainly in large installations where many nodes must be supported and distances between active repeaters are long. Typically, a transceiver box is physically connected to the Thick Ethernet backbone and a drop cable provides the actual connection to the LAN interface card present in the computer. The Thick Ethernet connection is actually a 15 pin Female D connector on the A2065 board. This physical interface is driven directly via transformer isolation by the Am7992B SIA. The transformers provide DC isolation and are designed to meet IEEE specifications. The function of the Am7992B is to decode/encode Manchester type serial data streams as per IEEE specifications for Ethernet. The key circuitry surrounding the Am7992B is the 20 MHz crystal (X1), which must meet exacting specifications, and the 5600 pF VCO Phaselock loop filter capacitor (C34). AMD data sheets call for a 5000 pF capacitor, but information from AMD applications engineers indicates that a value up to 6800 pF should be acceptable. Currently, this part is specified at 5600 pF ± 10% or better. Specifications for the 20 MHz crystal are set forth in the data sheet for the Am7992B. The jumper JP7 is supposed to affect the output signal for 802.3 applications. This jumper requires further testing and may need to be deleted for production. Thick Ethernet requires a +12V, 0.750A supply. This is supplied directly from the Amiga expansion connector. Note that a fuse is provided to protect against short circuits which might damage the Amiga or associated peripherals.

The second type of media is Cheapernet, commonly referred to as "Thin Ethernet" or 10Base2. Cheapernet evolved as a result of media costs associated with Thick Ethernet. Cheapernet allows for a "Bus" topology with up to 100 nodes. Inexpensive RG58 coax is used along with BNC T connectors and terminators. The Cheapernet section is comprised of the AM7996, a +5V to 9V DCDC converter, and various passive components which differentially drive the coax media and also act to recover the incoming data stream. The Cheapernet section also implements collision detection for collisions occurring on the media. Refer to the AM7996 data sheets for a complete technical discussion of the operation of the Cheapernet transceiver.

AUTOCONFIG LOGIC AND CONFIGURATION LOGIC

Autoconfiguration is accomplished by reading the 256*4 AutoID Prom and relocating the physical base address of the Ethernet board within some 64K of Amiga I/O memory space. The autoconfig logic is implemented in the 16L8A PAL along with the Prom, the 74F521 address comparator, and the 74LS373 address latch. When the Ethernet board is ready for autoconfiguration, its _CONFIGIN line is brought low, address 0xE80000 is decoded, and a board select is generated. During the configuration process, the Prom parameters are read into memory to create the necessary system structure for the configed devices. It should be noted that the board serial number is used to generate the board's physical Ethernet address. The signal _IDP is generated from the 16L8A PAL to decode the Prom chip select. The read signal _RD to the Prom is generated from the 20L8A PAL. Refer to the PAL equations for details. Once the Prom has been read, the Amiga will write to address 0xE80048 to load the onboard address latch. The Ethernet board will generate a write pulse called SATL to load a 74LS373 with the board's new base address. The SATL signal comes from the 16L8A PAL. It is generated from a decode of 0xE80000 and a write strobe called _SWR. The _SWR strobe comes from the 20R6A PAL. It is essentially a delayed write pulse using delayed AS and the 7M Amiga clock. Once the latch is written, _CONFIGOUT is generated, enabling the output buffer of the 74LS373 latch. The board is now relocated and will respond to its new address.

BUS CONTROL BUFFERS AND CONTROL LOGIC

The Ethernet board data path consists of a 16 bit (D15:D0) wide data bus and is used for reading and writing the Ethernet local memory and the Am7990 registers. Only 4 bits (D15:D12) are significant with respect to the AutoID Prom. Referring to Figure 1, a pair of 74LS245 and 74LS244 isolate the Amiga's system bus from the internal Data/Address paths. Only the Amiga 68000 or the Am7990 can have access to this internal data/address path at one time. Normally, the Am7990 is burst DMA reading or writing the 32K memory as packets are being received or transmitted. The host 68000 requests access to this internal bus to either read/write memory or Am7990 registers. The 68000 accesses are arbitrated based on the Am7990 requiring the bus. A wait state is inserted to guaranty meeting 60ns _AS to XRDY delay during arbitration time. The bus control function is implemented by the 20R6A PAL. This PAL generates the data bus transceiver control _DBE. This signal is active when there is no exceptional conditions and a signal _ABE is active. _ABE is active only when the Am7990 is not requesting the internal bus (_HOLD, _LANCE not asserted). This satisfies the condition that a mutually exclusive relationship exists between the 68000 and the Am7990. The Ethernet board also listens on _BERR for bus faults; if _BERR is ever active, _DBE will not be active. The signal _LANCE is generated to enable the LS244 buffers which pass the Am7990 DMA address thru to the Ram buffers. _LANCE in conjunction with _ABE determines which source (68000 or Am7990) drives the internal address path. The Am7990 works in a multiplexed address/data method. First an address is latched during the first part of the read/write cycle, then the actual data transfer occurs.

ONBOARD CONTROL LOGIC/BUFFERING

The onboard control logic consists mainly of chip selects and read and write strobes to memory and the Am7990. The 32K buffer is partitioned into a high bank and a low bank of 8K * 16 bits each. Address line A14 determines which bank is active. The read and write strobes to the memory are qualified by bus control signals. During 68000 R/W cycles, the signals READ, _UDS, and _LDS are used from the system bus along with _BSEL to control reading data. These same signals plus one generated onboard called _ENDCYC are used to generate write pulses. _ENDCYC is generated by the 20R6A PAL. During Am7990 bus ownership, a different set of signals controls the R/W timing pulses. All these control signals are generated within the 20L8A Internal Bus Control PAL. The 20L8A PAL also generates chip selects for the 32K memory and Am7990 I/O register. For further information, refer to the PAL equations and the Am7990 data sheet.

LOW LEVEL INTERFACE PROGRAMMING

For a complete discussion of programming the Ethernet board, refer to the Am7990 application sheets and the Ethernet device driver source. A brief explanation is given here. The Amiga configures the board and builds a config structure in memory. The Ethernet software goes out and finds the location of the board and reads the serial number. The serial number plus the manufacturer base Ethernet address make up the complete Ethernet address. The software then sets up the initialization block in the 32K memory which sets up two circular linked list buffers, one transmit and one receive queue. The initialization block refers to these queues as "descriptors". The Am7990 is then programmed via I/O transfers into internal registers for various network and operational parameters, along with the setting up of an interrupt handler. Finally, the action starts. The network layer software fills buffers to transmit, while emptying buffers that are filled from incoming packets.

A2065 ETHERNET BOARD MEMORY MAP

Amiga Address	Size	Usage
xx0000	256 bytes	Autoconfig Prom Contains standard autoconfig data and Ethernet address. Upper data byte only, i.e. D15-D12. Readable before and after autoconfig.
xx4000	4 bytes	LANCE Ethernet controller chip xx4000 Register address port (RAP) xx4002 Register data port (RDP)
xx8000	32K bytes	32K Packet Buffer

Notes: xx denotes upper address after autoconfiguration location (initially base board address appears at hex E80000).

The Autoconfig Prom is read only. It lies on data lines D15-D12. The serial number portion is used to hold the user specific portion of the Ethernet address. This partial address is concatenated with the vendor portion of the Ethernet address to form a full 6 byte address.

The Register Data Port and Register Address Port are defined in the Am7990 data sheets.

The 32K buffer is organized as 16K by 16 bits for word/byte, read/writes. This buffer is managed and initialized as per the Am7990 LANCE data sheets.

The board is decoded into two 16K chunks and one 32K chunk. Total size is 64K.

A2065 ETHERNET BOARD JUMPERS

When the shunt plug is inserted into a jumper position, the corresponding signal is active.

Interrupt Jumpers

JP1 INT1
JP2 INT2 (default setting)
JP3 INT4
JP4 INT5
JP5 INT6
JP6 INT7

Am7992 Transmit Mode Jumper

JP7 Transmit mode select. Default is to leave shunt plug out. See the Am7992 data sheets for actual usage.

Thick Ethernet/Cheapernet Jumper Block

ABC When the AB jumper is connected with the shunt block, Cheapernet is selected; otherwise, the connection of the BC jumper will select Thick Ethernet.

ENVIRONMENTAL TEST REQUIREMENTS

Units shall comply with the following environmental resistance requirements.

TEMPERATURE	
Operational	5 to 55°C
Storage	−20 to +70°C
Gradient	+10°C/hour
Temperature Cycle	−20 to 60° C, 10 cycles, 10 minutes minimum at each extreme, 5 minutes maximum between extremes
HUMIDITY	
Operational (relative)	10 to 90% (non-condensing)
Storage (relative)	5 to 95% (non-condensing)
VIBRATION	
Non-operating (randomfrequency)	5.2 Gs per MIL-STD 202 Method 214, 15 min. in each of three axes
SHOCK	
Operational	5 Gs to each of 6 axes, two 11 mSec half sinewave shocks
Non-Operational	20 Gs applied as above
ALTITUDE	
Operational	0 to 3,000 meters
Non-Operational	0 to 15,000 meters

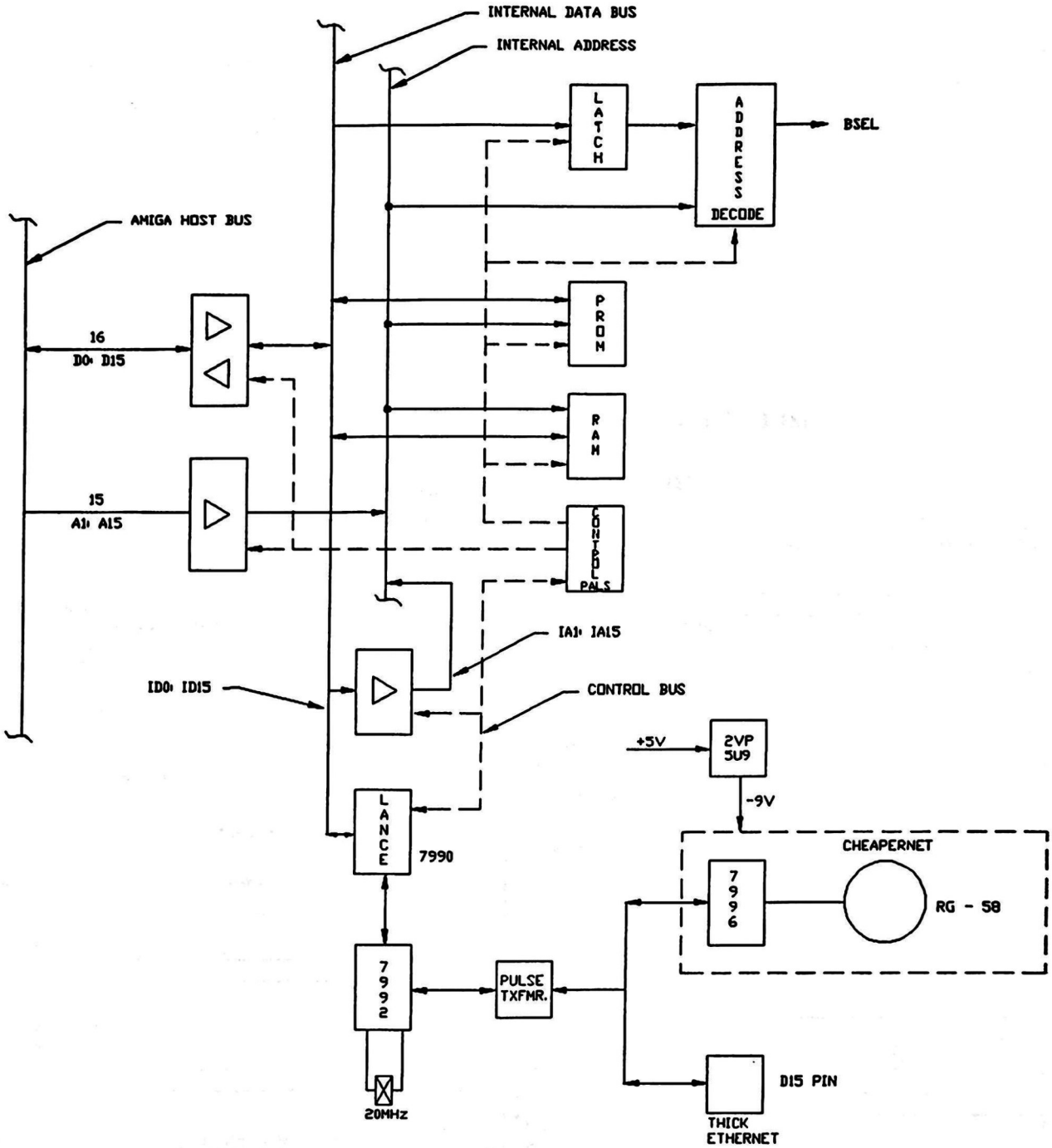

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM

Commodore International Spare Parts List
SHIPPING ASSEMBLIES

Commodore part numbers are provided for reference only and do not indicate the availability of spare parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Part number information may vary according to country, some parts may not be available in all countries.

532065-01	A2065 SHIPPING ASSY
363097-06	BOX INDIVIDUAL PACKING
363035-05	BOX BULK SHIPPING
363361-01	MANUAL USERS GUIDE ENGLISH
314877-04	SERVICE CENTER LIST
318290-01	WARRANTY CARD
318928-01	ANTI STATIC BAG
313430-01	PCB ASSY

Commodore International Spare Parts List
PCB Components
PCB Assembly #313430-01

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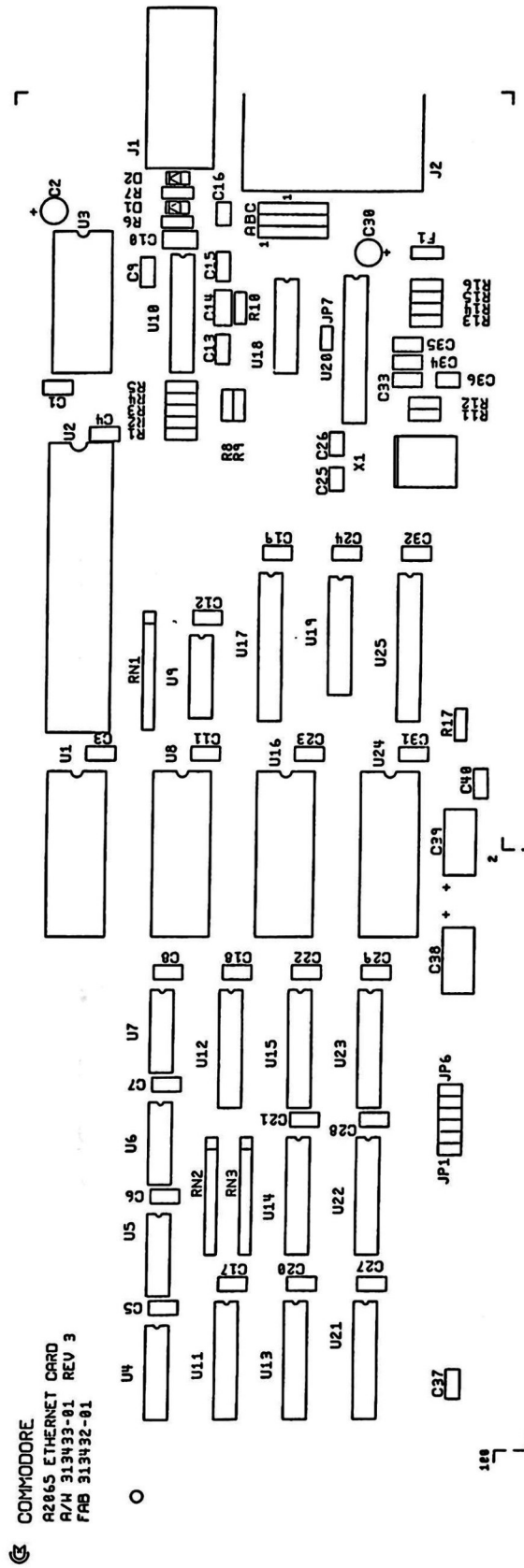
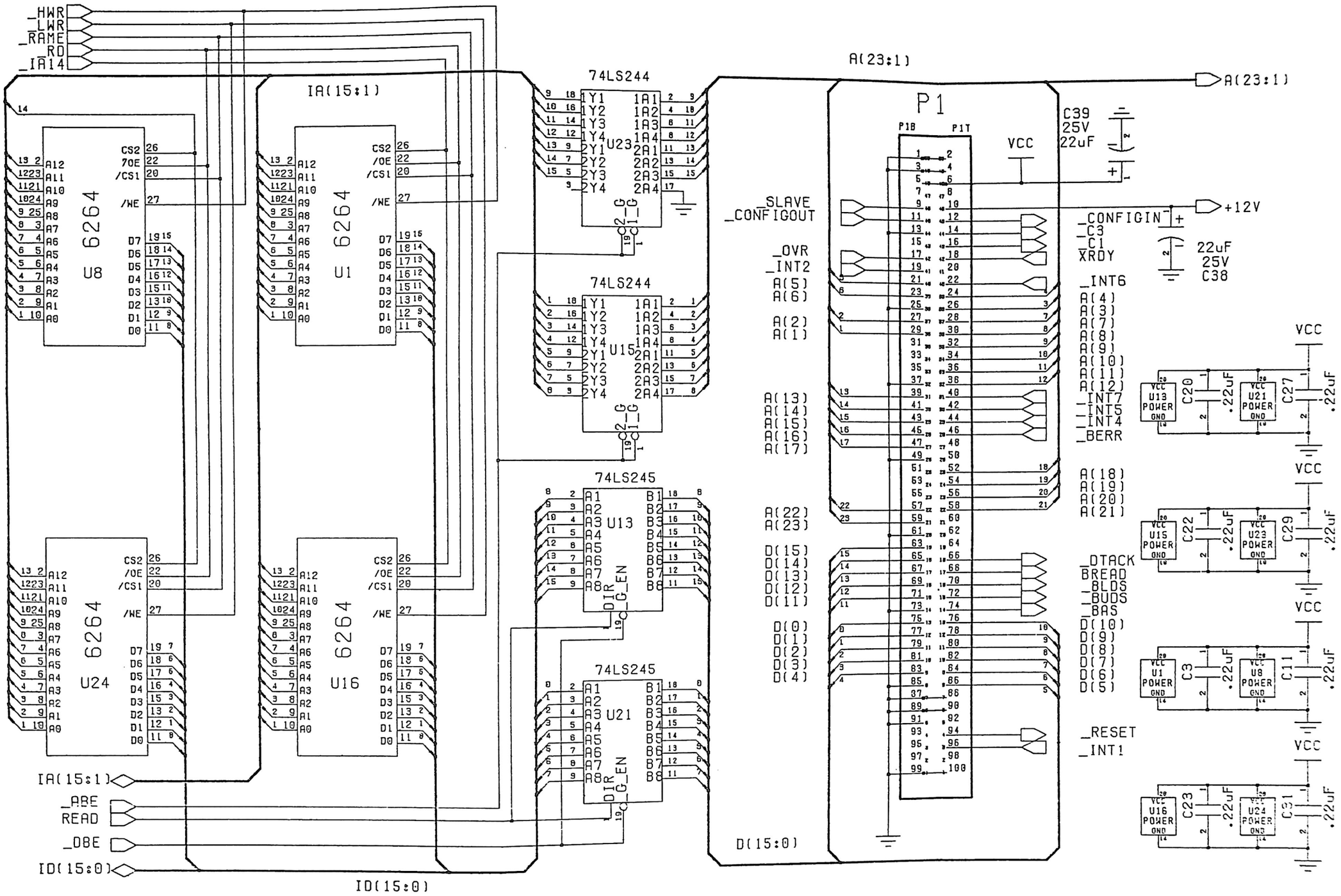
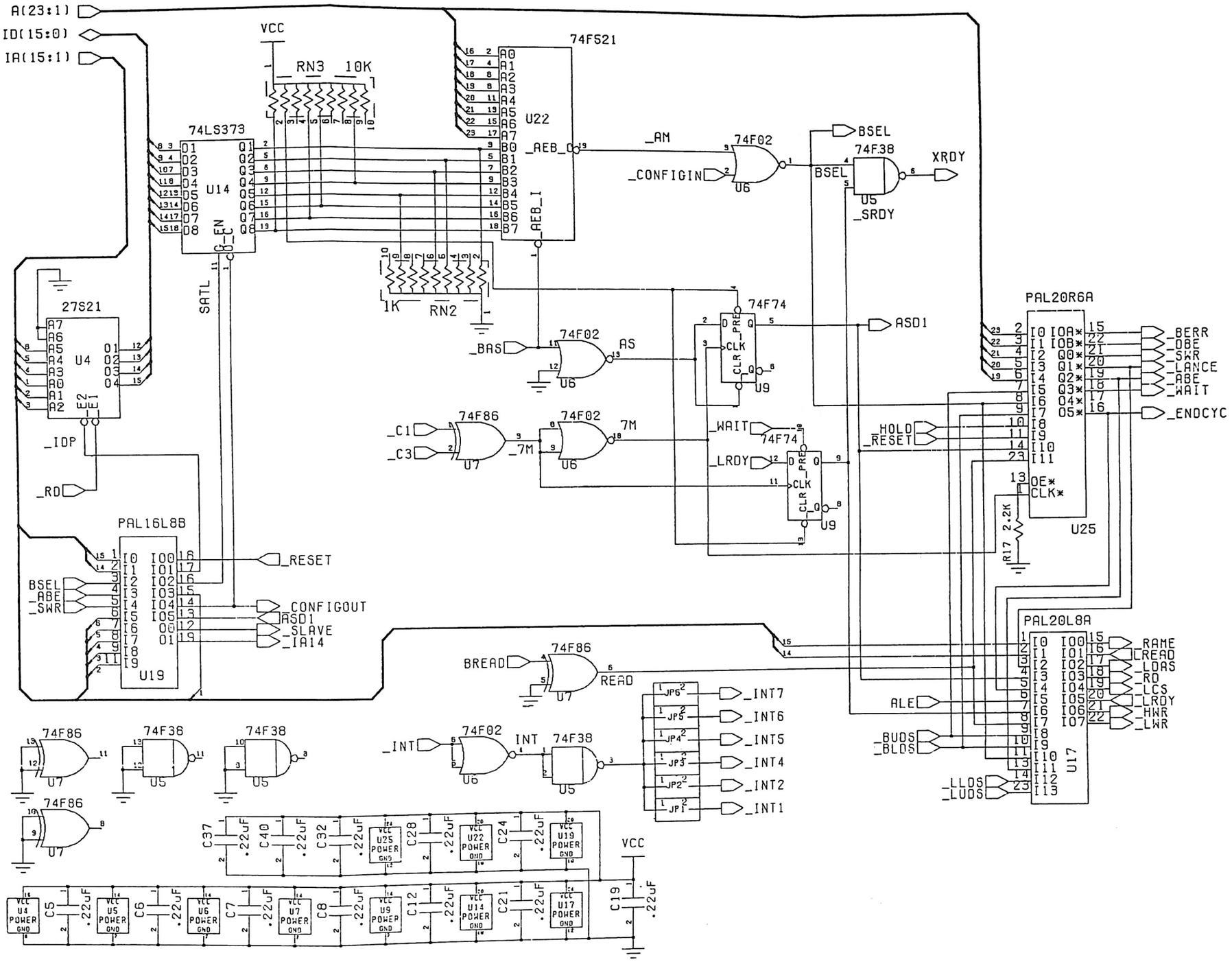
IC COMPONENTS		
313430-01	PCB ASSY A2065 ETHERNET LAN CARD	
390586-01	74F38	U5
390092-01	74F02	U6
390198-01	74F86	U7
901521-29	74LS373	U11,U12,U14
901521-46	74LS245	U13,U21
901521-13	74LS244	U15,U23
318041-01	74F521	U22
390081-01	74F74	U9
390631-01	LSI AMD7990 LANCE	U2
390632-01	AMD7992B SIA	U20
390633-01	AMD7996 TRANSCEIVER	U10
390636-01	20L8A INTERNAL BUS CONTROL PAL	U17
390637-01	20R6A BUS CONTROL PAL	U25
390638-01	16L8B CONFIG PAL	U19
390639-01	PROM 256X4 AUTOCONFIG A2065	U4
310024-01	8K X 8 SRAM 150 NS	U1,U8,U16,U24
390640-01	LIN DC - DC CONV +5V TO −9V	U3
390641-01	TRANSFORMER PULSE 75 UH	U18
390642-01	CRYSTAL 20MHZ HC - 49/U	X1
IC SOCKETS		
904150-05	L/P 28 PIN DIP .600	U1,U8,U16,U24
904150-02	L/P 16 PIN DIP .300	U4
251313-01	DIP 48 PIN .600	U2
390060-01	DIP 24 PIN .300	U17,U20,U25
904150-08	L/P DIP 20 PIN .300	U10,U19
RESISTOR NETWORKS		
902410-07	SIP 10K OHM 10 PIN	RN1,RN3
902410-10	SIP 1K OHM 10 PIN	RN2
RESISTORS 1% @ ¼ WATT, UNLESS OTHERWISE SPECIFIED		
251575-55	METAL 40.2 OHM	R2,R3,R13-R16
251575-58	METAL 510 OHM	R11
251575-39	METAL 3K	R12
251575-54	METAL 9.09 OHM	R5,R7
251575-62	METAL 150K OHM	R1
251575-46	METAL 174 OHM	R4
251575-57	METAL 499 OHM	R8
251575-60	METAL 24.9K OHM	R9
251575-61	METAL 75K OHM	R10
251575-35	METAL 1K OHM	R6
901550-18	CF 2.2K OHM, ¼ WATT, 5%	R17

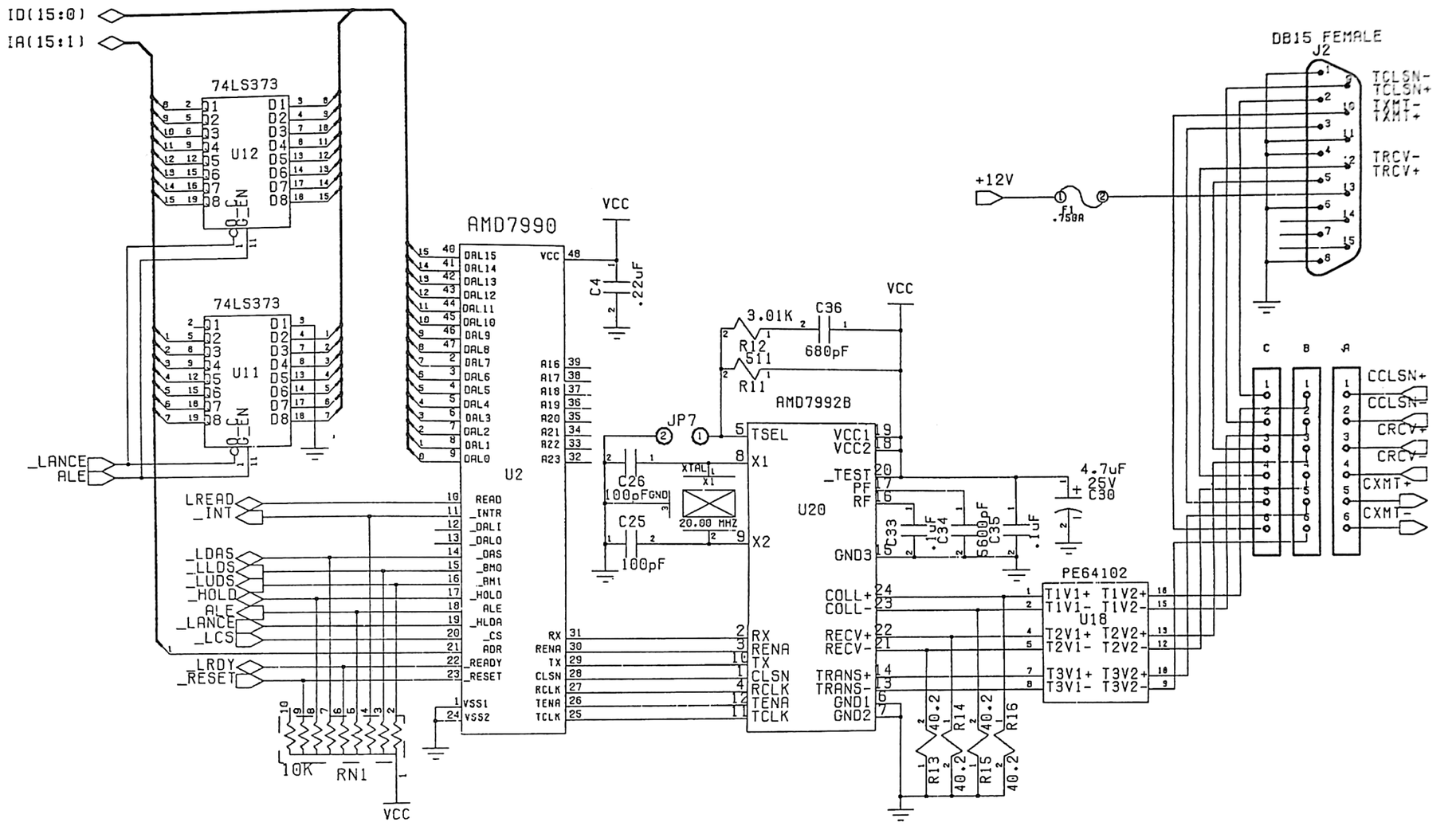
CAPACITORS		
900020-08	CER RDL .22UF 100V	C3-C8,C11,C12,C17-C24, C27-C29,C31,C32,C37, C40
900014-08	CERM RAD .1 UF MLC X7R	C1,C13,C15,C33,C35,C9
900019-15	CERM RAD 100PF MLC NPO	C25,C26
900050-28	MICA RAD 47PF NPO	C10
900019-12	CERM RAD MLC 680PF NPO	C36
900019-33	CERM RAD MLC 5600PF NPO	C34
900019-34	CERM RAD MLC 220PF NPO	C16
390646-01	CERM RAD MLC 5.0 PF NPO	C14
900101-08	ELEC AXL 22 UF 25V	C38,C39
900402-08	TANT RAD 4.7UF 25V	C30
900402-13	TANT RAD 1.0 UF 35 V	C2
CONNECTORS		
390584-02	PCB MOUNT RT/ANGLE FEMALE BNC	J1
390241-09	15 PIN DSUB RT/ANGLE FEMALE	J2
903345-06	HEADER DIL 12 PIN .100	JP1-JP6
903326-02	HEADER DIL 2 PIN .100	JP7
390043-01	SHUNT FEMALE 2 POS	JP2
390043-02	SHUNT FEMALE DIL .100 12 POS	ABC
390043-01	SHUNT FEMALE 2 POS (SUBSTITUTE FOR 390043-02)	ABC
313429-01	ETHERNET CARD BRACKET	
DIODES		
900750-02	1N4002	D1
390645-01	1N4150	D2
390280-03	FUSE .750A PICO	F1
MISCELLANEOUS		
316893-01	LABEL FCC ID A2065	
366189-01	LABEL COPYRIGHT	



PCB BOARD LAYOUT #313433, REV. 3


_HWR
_LWR
_RAME
RD
_IA14
IA(15:1)
A(23:1)
74LS244
U23
U15
74LS245
U13
U21
6264
U8
U1
U24
U16
P1
P1B
P1T
VCC
C39
25V
22uF
+12V
_CONFIGIN
_C3
_C1
XRDY
22uF
25V
C38
_SLAVE
_CONFIGOUT
_OVR
_INT2
A(5)
A(6)
A(2)
A(1)
A(13)
A(14)
A(15)
A(16)
A(17)
A(22)
A(23)
D(15)
D(14)
D(13)
D(12)
D(11)
D(0)
D(1)
D(2)
D(3)
D(4)
_INT6
A(4)
A(3)
A(7)
A(8)
A(9)
A(10)
A(11)
A(12)
_INT7
_INT5
_INT4
_BERR
A(18)
A(19)
A(20)
A(21)
_DTACK
BREAD
_BLDS
_BUDS
_BAS
D(10)
D(9)
D(8)
D(7)
D(6)
D(5)
_RESET
_INT1
C20
C27
C22
C29
C3
C11
C23
C31
.22uF
IA(15:1)
_ABE
READ
_DBE
ID(15:0)
D(15:0)


A(23:1)
ID(15:0)
IA(15:1)
VCC
RN3 10K
74LS373
U14
74FS21
U22
_AEB_O
_AEB_I
_AM
74F02
_CONFIGIN
U6
BSEL
74F38
U5
XRDY
_SRDY
1K
RN2
SATL
27S21
U4
_IDP
_RD
_BAS
AS
74F74
U9
ASD1
PAL20R6A
U25
_BERR
_DBE
_SWR
_LANCE
_ABE
_WAIT
_ENDCYC
R17 2.2K
74F86
U7
_C1
_C3
_7M
74F02
7M
_WAIT
_LRDY
_HOLD
_RESET
PAL16L8B
U19
_RESET
BSEL
_ABE
_SWR
_CONFIGOUT
ASD1
_SLAVE
_IA14
BREAD
READ
PAL20L8A
U17
_RAME
LREAD
_LDAS
_RD
_LCS
_LRDY
_HWR
_LWR
ALE
_BUDS
_BLDS
_LLDS
_LUDS
_INT
INT
_INT7
_INT6
_INT5
_INT4
_INT2
_INT1
JP6
JP5
JP4
JP3
JP2
JP1
C37 .22uF
C40 .22uF
C32 .22uF
C28 .22uF
C24 .22uF
C5 .22uF
C6 .22uF
C7 .22uF
C8 .22uF
C12 .22uF
C21 .22uF
C19 .22uF
U3 POWER
U5 POWER
U6 POWER
U7 POWER
U9 POWER
U14 POWER
U17 POWER
U19 POWER
U22 POWER
U25 POWER
GND


ID(15:0)
IA(15:1)
74LS373
U12
74LS373
U11
OE
_EN
_LANCE
ALE
AMD7990
U2
VCC
C4
.22uF
DAL15
DAL14
DAL13
DAL12
DAL11
DAL10
DAL9
DAL8
DAL7
DAL6
DAL5
DAL4
DAL3
DAL2
DAL1
DAL0
A16
A17
A18
A19
A20
A21
A22
A23
LREAD
_INT
_LDAS
_LLDS
_LUDS
_HOLD
ALE
_LANCE
_LCS
LRDY
_RESET
READ
_INTR
_DALI
_DALO
_DAS
_BM0
_BM1
_HOLD
ALE
_HLDA
_CS
ADR
_READY
_RESET
VSS1
VSS2
RX
RENA
TX
CLSN
RCLK
TENA
TCLK
10K
RN1
VCC
3.01K
R12
511
R11
C36
680pF
AMD7992B
JP7
TSEL
X1
XTAL
C26
100pF
GND
C25
100pF
20.00 MHZ
X2
VCC1
VCC2
_TEST
PF
RF
GND3
U20
4.7uF
25V
C30
C33
.1uF
C34
5600pF
C35
.1uF
COLL+
COLL-
RECV+
RECV-
TRANS+
TRANS-
GND1
GND2
PE64102
U18
T1V1+
T1V1-
T1V2+
T1V2-
T2V1+
T2V1-
T2V2+
T2V2-
T3V1+
T3V1-
T3V2+
T3V2-
R13
40.2
R14
40.2
R15
40.2
R16
40.2
+12V
F1
.750A
DB15 FEMALE
J2
TCLSN-
TCLSN+
TXMT-
TXMT+
TRCV-
TRCV+
C
B
A
CCLSN+
CCLSN-
CRCV+
CRCV-
CXMT+
CXMT-
J1
J1
J2
J2
T1
T2
VCC
C17
.22uF
C18
.22uF
U11 POWER
U12 POWER
GND

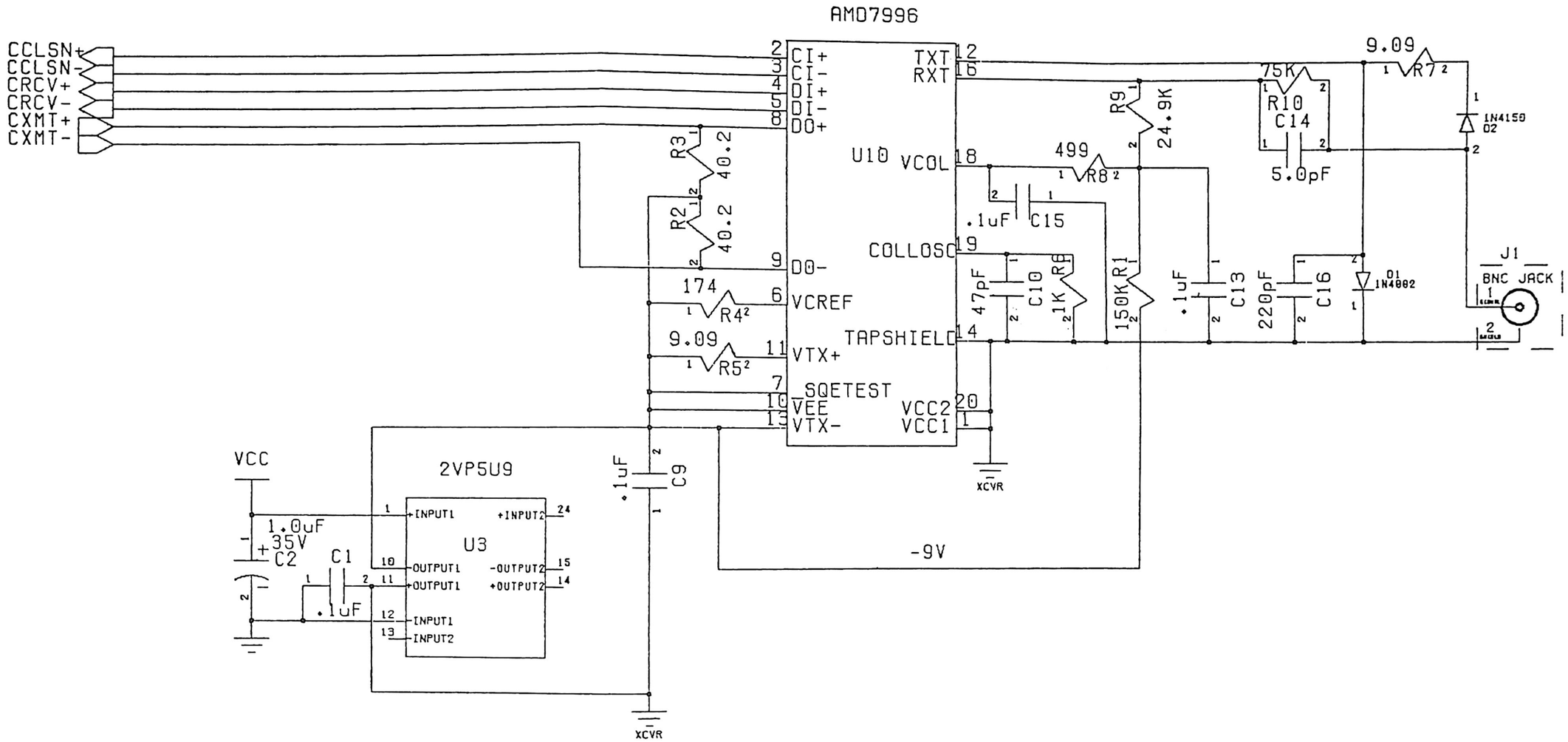

AMD7996
CCLSN+
CCLSN-
CRCV+
CRCV-
CXMT+
CXMT-
CI+
CI-
DI+
DI-
DO+
DO-
VCREF
VTX+
SQETEST
VEE
VTX-
TXT
RXT
VCOL
COLLOSC
TAPSHIELD
VCC2
VCC1
U10
R3 40.2
R2 40.2
174 R4
9.09 R5
499 R8
R9 24.9K
R10 75K
C14 5.0pF
9.09 R7
1N4150 D2
.1uF C15
47pF C10
1K R6
150K R1
.1uF C13
220pF C16
D1 1N4002
J1 BNC JACK
XCVR
VCC
2VP5U9
1.0uF +35V C2
C1 .1uF
.1uF C9
INPUT1
+INPUT2
U3
OUTPUT1
-OUTPUT2
+OUTPUT2
-9V

TABLE OF CONTENTS

- **SPECIFICATIONS**
- **PARTS LISTS**
- **SCHEMATICS**

A2232 MULTIPORT SERIAL CARD
FUNCTIONAL SPECIFICATION

DESCRIPTION

The A2232 Multiport Serial Card is a standard 100 pin Zorro II expansion card for the Amiga 2000. It provides the Amiga with 7 additional standard RS232 serial ports, capable of speeds up to 19.2 kbaud. For more serial channels, additional A2232 boards can be plugged into the system at the same time.

SERIAL PORTS

All 7 of the serial ports are available at the rear of the board via 7 8-pin mini DIN connectors. The board comes with 7 short adapter cables which can be plugged into each of these connectors, which provides a more standard DB-25 connection.

signal	8 pin mini DIN	DB-25	dir
TxD / RxD	1	2	out/in
RxD / TxD	2	3	in/out
Request to Send (RTS)	3	4	out
Clear to Send (CTS)	4	5	in
Data Set Ready (DSR)	5	6	in
Signal Ground	6	7	
Data Carrier Detect (DCD)	7	8	in
Data Terminal Ready (DTR)	8	20	out

In order to simplify connections, the transmit data (TxD) and receive data (RxD) signals can be swapped on the A2232 board. There is an 8 jumper block (JB1) at the back of the board which makes this possible. Each of the 7 serial channels is associated with 4 possible jumper locations, and uses 2 of the jumpers. Figure 1 shows the schematic for this jumper block. Figure 2 shows how to configure the shorting blocks for a single channel.

All unused inputs have pullups on the board which keeps them at their 'TRUE' value if not connected. This greatly simplifies things if you are only using a 3-wire connection.

A2232 SYSTEM CONFIGURATION

The A2232 expansion card conforms to the auto-config protocol.

auto-config size	64k bytes
manufacturer code	202 (hex)
product number	46 (hex)

A block diagram of the board is shown in figure 3.

An 8 bit processor was incorporated in the A2232 in order to remove the burden of handling I/O from the Amiga system's main CPU. Also, since the Amiga is multi-tasking, it is impossible to ensure that the system's CPU can respond in a timely manner in order to service the needs of the I/O channels. The 8 bit processor used is a 65CE02, which is an enhanced version of the 6502, providing faster operation through new instructions and higher operating speeds.

The 6502 and the Amiga communicate mainly through the 16k bytes of shared RAM. The Amiga also has control over the 6502's *RESET and *IRQ signals. The 6502 can interrupt the Amiga via the *INT2 interrupt line. The Amiga must clear this interrupt itself.

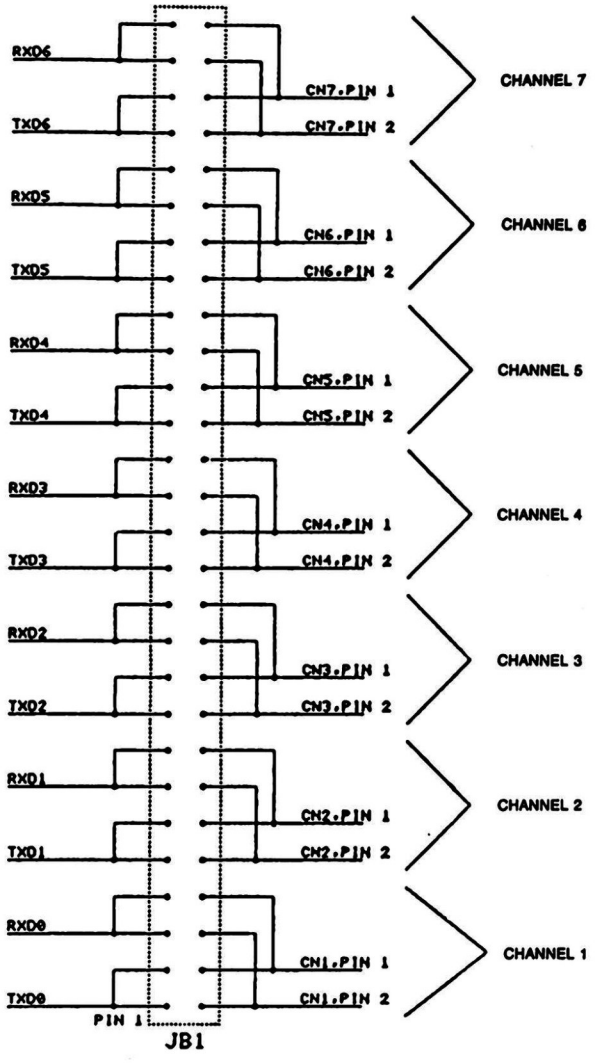


FIGURE 1 — JUMPER BLOCK SCHEMATIC

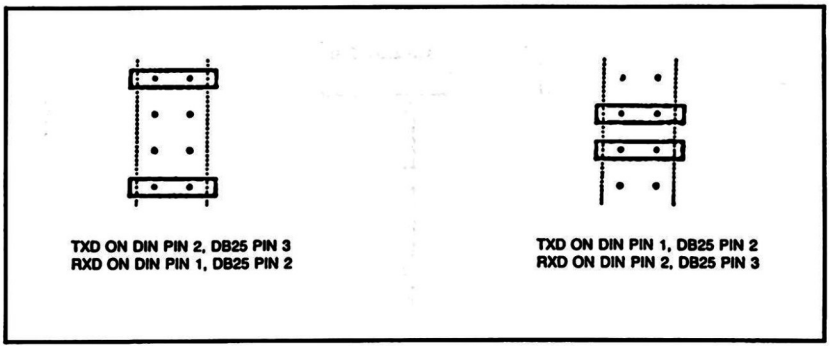


FIGURE 2 — OPTIONS FOR CONNECTING TXD & RXD FOR EACH CHANNEL

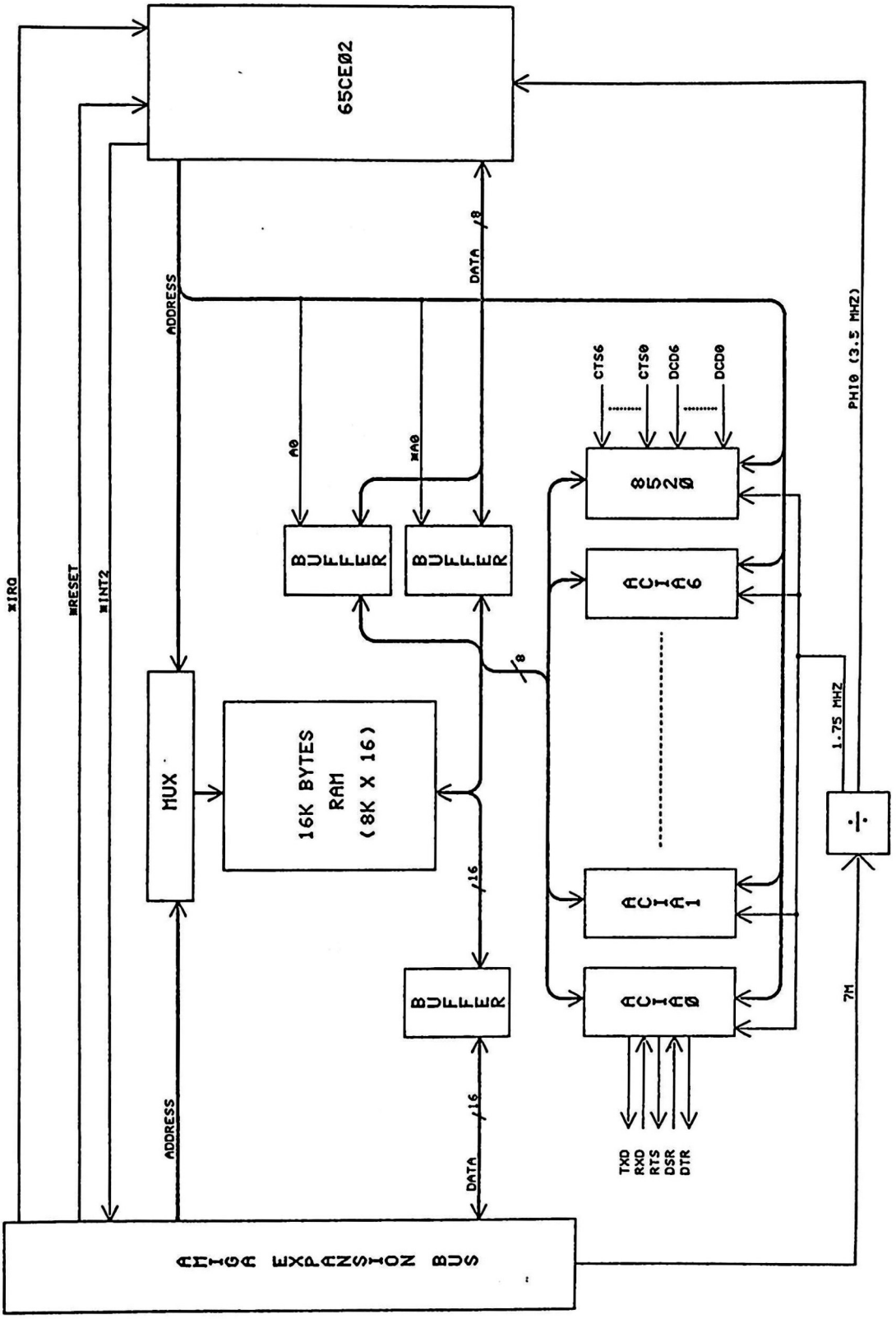


FIGURE 3 — A2232 SYSTEM BLOCK DIAGRAM

board offset	description
$0000-$3FFF	16k bytes of shared RAM
$4000	reset the *INT2 interrupt caused by the 6502
$8000	set 6502's *RESET line low
$A000	set 6502's *IRQ line low
$C000	set 6502's *RESET line high

AMIGA's MEMORY MAP OF A2232

The control signals listed above are affected when the Amiga does an access (read or write) to the locations listed. No information is passed over the data bus.

The 6502 executes code which is downloaded by the Amiga into shared RAM. When the Amiga goes through a hardware reset, the *RESET line to the 6502 is latched low, keeping it frozen. This gives the Amiga a chance to download the code which the 6502 is to execute. After the code is downloaded, the 6502 is started when the Amiga does a dummy access at board offset of $C000, allowing the *RESET line to go high. The Amiga can freeze the 6502 at any time later by accessing location $8000, latching the *RESET line low again. More or different code may now be loaded, and the 6502 restarted again.

The 6502 has control over all 7 of the 6502 ACIAs. The Amiga cannot access them directly.

address	description
$0000-$3FFF	16k bytes of shared RAM
$4400	ACIA for channel 1
$4C00	ACIA for channel 2
$5400	ACIA for channel 3
$5C00	ACIA for channel 4
$6400	ACIA for channel 5
$6C00	ACIA for channel 6
$7000	set Amiga's *INT2 interrupt low
$7400	ACIA for channel 7
$7C00	8520 CIA
$8000	Reset (set high) the *IRQ caused by the Amiga
$C000-$FFFF	16k bytes of shared RAM

6502's MEMORY MAP OF THE A2232

Note that 16k of RAM appears to the 6502 in 2 places. This was done so that the 6502's 'zero page' of memory and the reset vectors could be handled with the same RAM.

A2232 System Timing

The 7 Megahertz clock coming from the Amiga is used to drive a state machine that generates the clocks used on the A2232. The PHI0 clock which drives the 6502 is divided down from the 7M clock. Normally, the 6502 runs at 3.5 Mhz. However, so that the board can use the less expensive 2 Mhz 6551's, the 6502 must slow down to 1.75 Mhz when accessing the ACIA's (6551's). Since the 6551's are provided with a constant 1.75 Mhz clock, the 6502 must first sync up with the 6551's clock before completing the access. The 6502 is also slowed down while the Amiga accesses the shared RAM. This is done by keeping the PHI0 clock low while the 68000 accesses the RAM, effectively halting the 6502.

Figure 4 illustrates the operation of the state machine. Each of the states is 1 7M cycle long (140 nanosecs). The arrows connecting each of the states are numbered as different transitions.

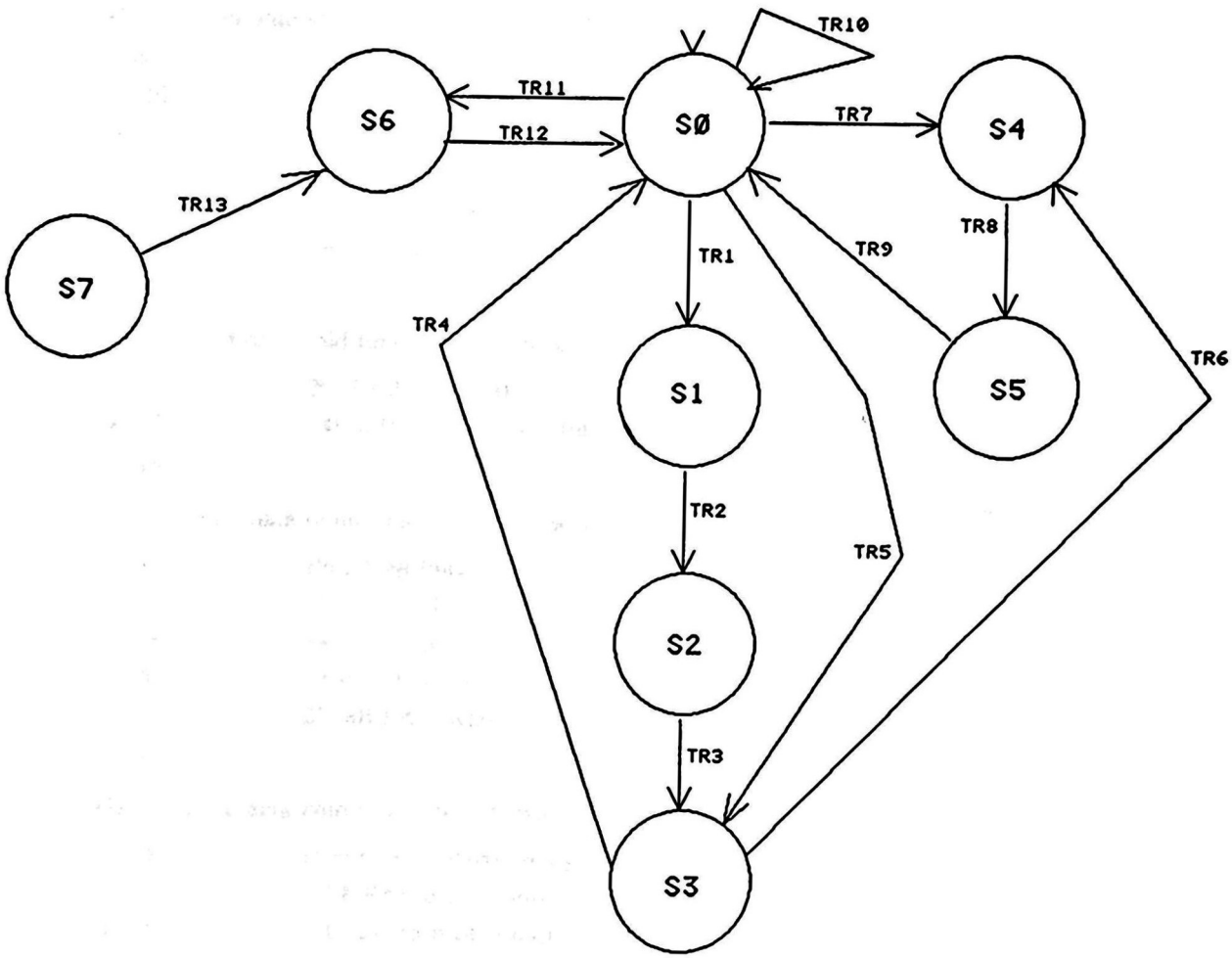


FIGURE 4 — A2232 STATE MACHINE DIAGRAM

6502 RAM ACCESS

The 6502 accesses ram during states S0 and S3. If it is determined during S0 that the 6502 wants to access the RAM, TR5 is used, bypassing S1-S2. The Phi0 clock is low during S0, and goes high during S3, yielding the 3.5 Mhz clock. At the end of S3, there are 2 different transitions that can be taken. TR4 is taken if the 68000 is not waiting to access the RAM. If the 68000 is waiting to get at the RAM, but is not properly synched with the C1 clock, TR4 is also taken. TR6 is taken when the 68000 is waiting, and is properly synched.

Referring to figure 5 ...

(7) read data setup time : > = 40 nsecs

280	Phi2 cycle time
− 50	6502 address setup time (max)
− 15	74F257 delay (max)
− 15	*CS goes low, 20L8B delay (max)
−100	RAM access time
− 18	74LS245 delay (max)
82	

(8) read data hold time : > = 10 nsecs

5	20L8B delay (min)
+ 5	74LS245 turn off time (min)
10	

(10) write data setup time : > = 50 nsecs

140	Phi2 high time
− 50	6502 write data delay (max)
− 18	74LS245 delay (max)
− 30	Phi0 to Phi2 delay (max)
+ 5	20L8B PAL delay (min)
47	

(11) write data hold time : > = 5 nsecs

5	Phi0 to Phi2 delay (min)
+ 5	20L8 PAL delay (min)
+ 5	74LS245 turn off (min)
15	

6502 ACCESSING 6551's

Since the 6551's can only run at 1.75 Mhz, they must be provided with a constant 1.75 Mhz (or less) clock. In order for the 6502 to access the 6551, it must slow down to this speed as well. During S0, the state machine determines that the 6502 wants to access a 6551. If the clock driving the 6551 is currently low, then the 6502 is in sync with the 6551 (the PHI0 clock is always low during S0). TR1 is taken and the access may continue. If the 6551 clock is high, then they are out of sync, and TR11 is taken. TR12 immediately follows TR11, during which the 6551 clock is inverted. The state machine now determines during S0 that they are in sync, and TR1 can be taken. PHI0 and the 6551 clock are both low during S1, and go high during S2 and S3, yielding 1.75 Mhz. At the end of S3 the same decisions as described at the end of a RAM access are again executed.

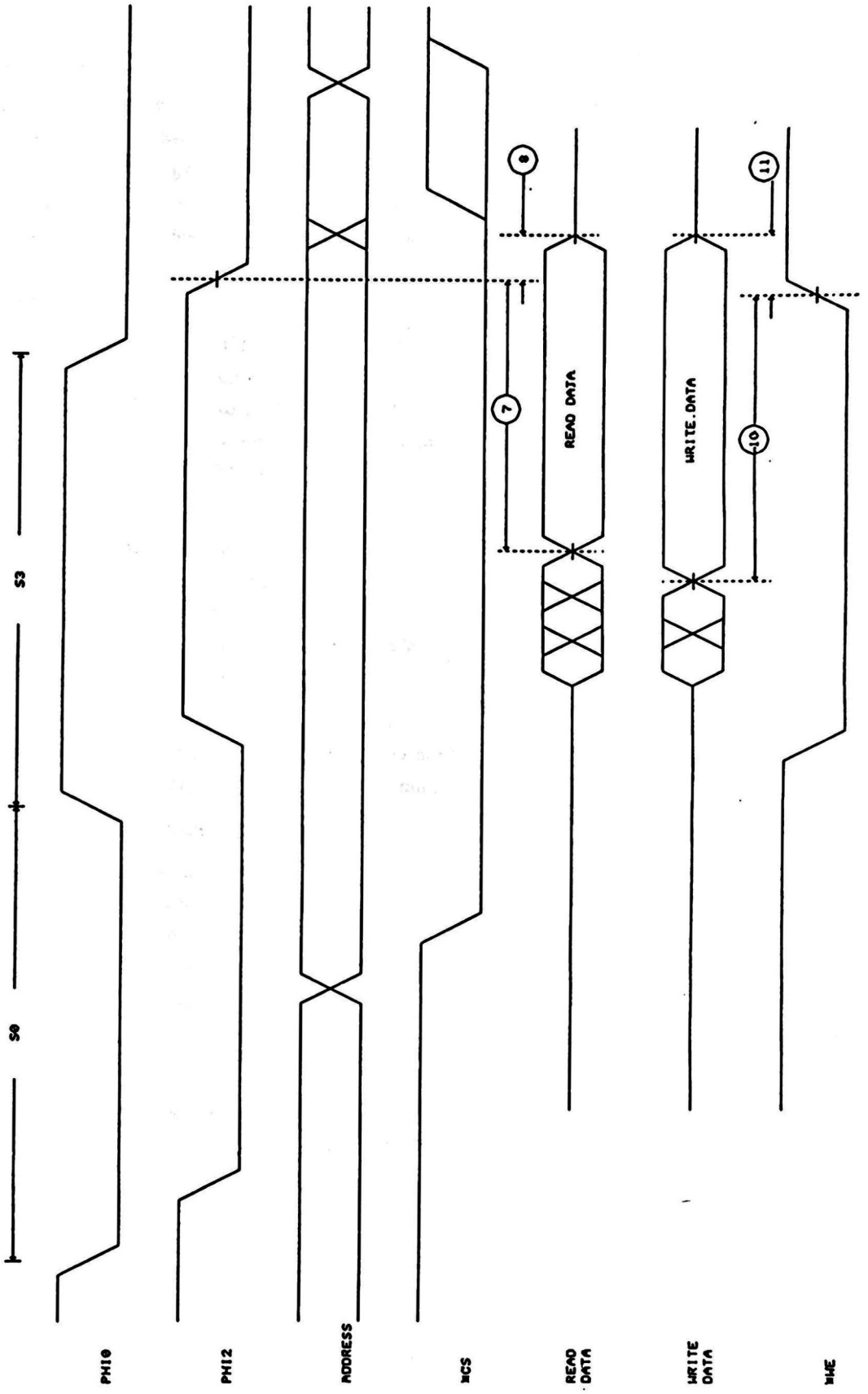


FIGURE 5 — 6502 RAM ACCESS

Referring to figure 6 ...

(1) setup time for ADR, RSO-3,R/W,CS,*CS : > = 70 nsecs

The latest of these signals is *CS.

280	6551 CLK low time
− 30	Phi0 to Phi2 delay (max)
− 40	6502 Address setup time (max)
− 30	74LS138 delay (max)
180	

(2) write data setup time : > = 60 nsecs

280	6551 CLK high time
− 30	Phi0 to Phi2 delay (max)
− 50	6502 write data setup time (max)
− 18	74LS245 delay (max)
182	

(3) write data hold time : > = 20 ns

5	Phi0 to Phi2 delay (min)
+ 5	20L8B delay (min)
+ 5	74LS245 turn off time (min)
15	(case 1)
5	Phi0 to Phi2 delay (min)
+ 5	6502 write data hold (tHD min)
+ 5	74LS245 in to out delay (min)
15	(case 2)

(4) read data setup time : > = 40 nsecs

280	Phi2 high time
+ 5	Phi0 to Phi2 delay (min)
−150	read data access of 6551 (max)
− 18	74LS245 delay (max)
107	

(5) read data hold time : > = 10 nsecs

5	20L8B delay (min)
+ 5	74LS245 turn off time (min)
10	

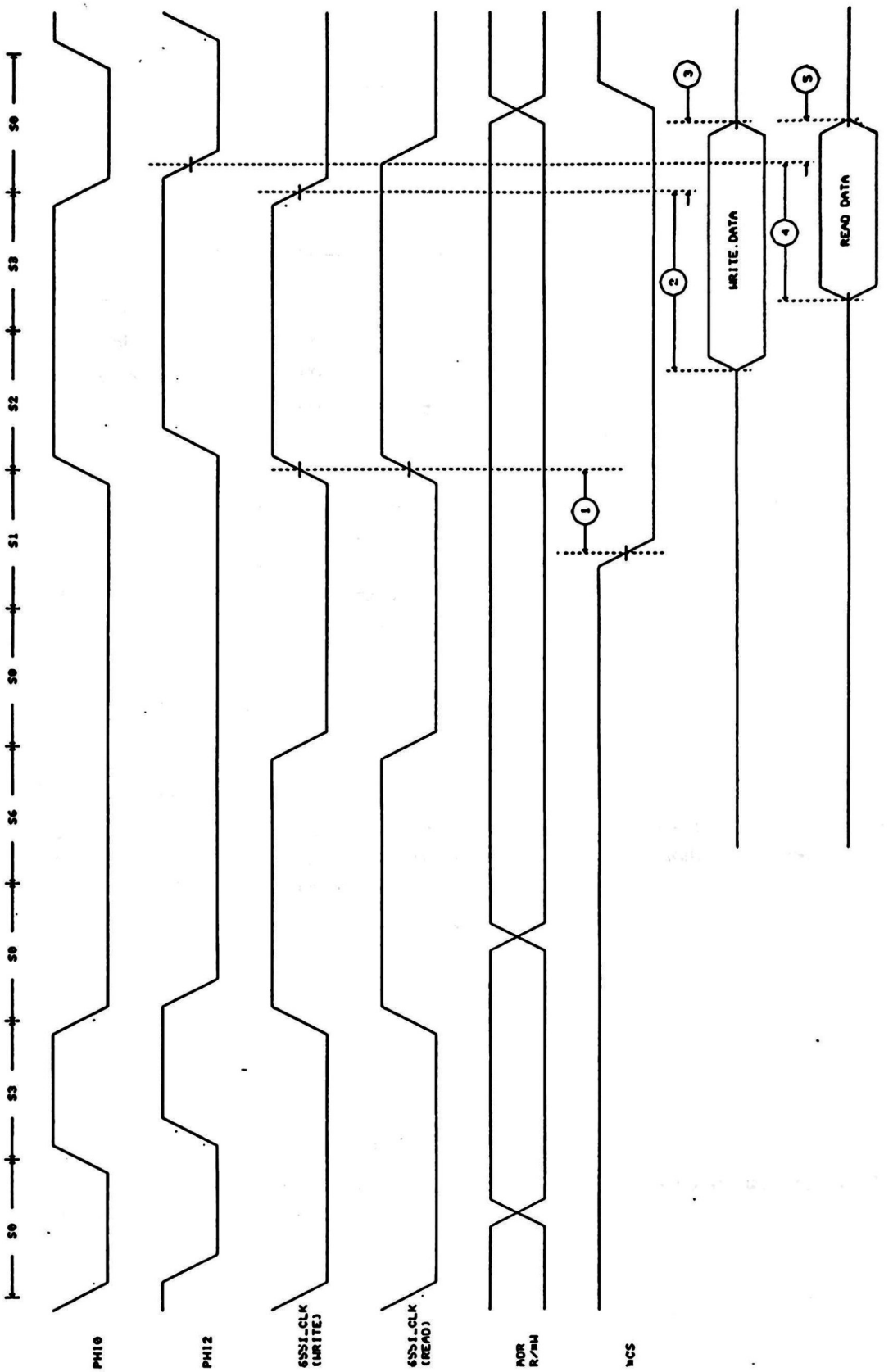


FIGURE 6 — ACCESSING 6551's

68000 RAM ACCESS

There are 2 states during which a 68000 request can be recognized. One of these is S3, which has already been described. During S0 a 68000 request can also be recognized. In both instances, the 68000 takes precedence. If the 68000 doesn't want access, then the 6502 is allowed to continue. During 68000 accesses the 6502 is halted by holding the Phi0 clock low. TR7 and TR6 both bring the state machine to S4, where the 68000 access is allowed to finish. From the time that the board is selected, it drives the override (*OVR) and *DTACK signals until the end of S5. As long as it may take for the state machine to get to S4, wait states are inserted into the 68000 access by keeping *DTACK high. At the beginning of S4 *DTACK goes low signalling to the 68000 that the access may be completed.

Referring to figure 7 ...

(15) read data setup time : > = 10 nsecs

referenced from the start of 68000 T4 ...

210	time from start of T4 to end of T6
− 15	Q delay of 16R8A PAL, Phi0 goes low (max)
− 30	Phi0 to Phi2 delay (max)
− 15	20L8B PAL delay, MUX goes low (max) (*RAMCS goes low too)
− 15	74F257 switching delay (max)
−100	RAM access time
− 10	74ALS245 delay (max)
− 18	74LS245 delay, on expansion bus (max)
7	

(16) read data hold time : > = 0

Obvious.

(17) write data setup time : > = 50 nsecs

Assume that C3 transitions coincident with the rising edge of the 7M clock. Referenced from the rising C3 at the beginning of T4, the RAM *WE goes high 140 ns later. Referenced from the same rising edge of C3, the data becomes valid:

15	Q delay of 16R8A PAL (max)
+ 35	20L8 PAL delay (max)
+ 7	74F32 delay (max)
+ 20	74ALS245 turn on time (max)
77 ns	

So, 140 − 74 = 66 ns

(18) write data hold time : > = 5 nsecs

The write pulse went away half way through S5. The data and addresses stay valid through the rest of S5, or approximately 70 nsecs.

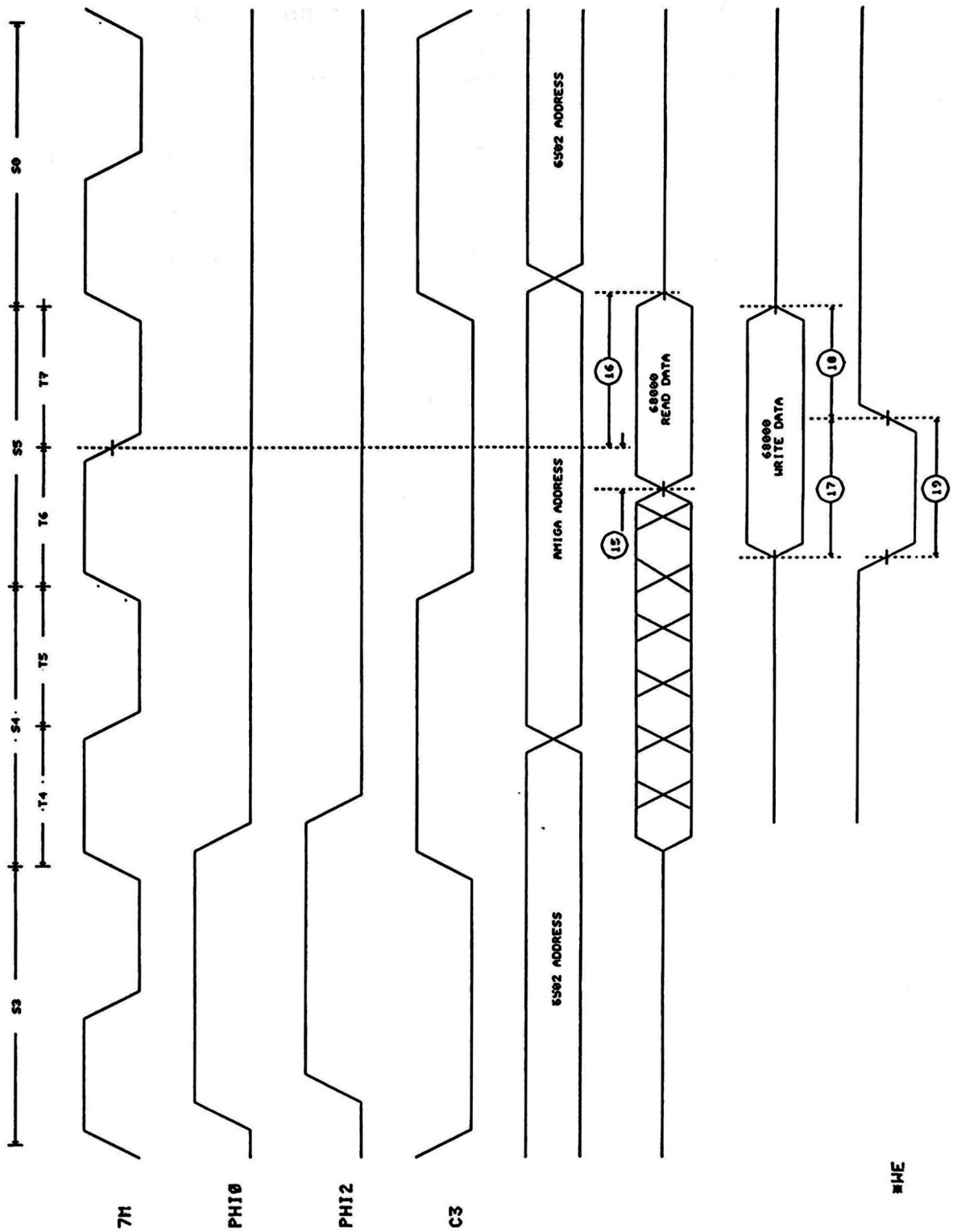


FIGURE 7 — 68000 RAM ACCESS

Commodore International Spare Parts List
SHIPPING ASSEMBLIES

Commodore part numbers are provided for reference only and do not indicate the availability of spare parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Part number information may vary according to country, some parts may not be available in all countries.

312859-01	A2232 SHIPPING ASSY (U.S.)
363128-01	BOX PACKING
363127-01	BOX BULK SHIPPING
363100-01	MANUAL, USERS (SUB)
363375-01	MANUAL, USERS EFIGS
314877-04	BOOKLET SERVICE CENTER LIST
312864-02	CABLE ASSY MINI DIN TO DB25 (QTY=7)
318290-01	CARD WARRANTY U.S.
318928-01	BAG ANTI STATIC
318896-01	S/W LICENSE AGREEMENT
317769-01	DISKETTE ASSY
318940-01	SPACER CARDBOARD
312860-01	PCB ASSY
318733-02	MANUAL AMIGATERM
312341-02	CARD DISK EXCHANGE

312859-02	A2232 SHIPPING ASSY (EFIGS)
363128-01	BOX PACKING
363127-01	BOX BULK SHIPPING
363100-01	MANUAL, USERS (SUB)
363375-01	MANUAL, USERS EFIGS
312864-02	CABLE ASSY MINI DIN TO DB25 (QTY=7) (CAN SUB to −01)
318928-01	BAG ANTI STATIC
317769-01	DISKETTE ASSY
318940-01	SPACER CARDBOARD
312860-01	PCB ASSY
318733-02	MANUAL AMIGATERM

312859-03	A2232 SHIPPING ASSY (CANADA)
363128-01	BOX PACKING
363127-01	BOX BULK SHIPPING
363100-01	MANUAL, USERS (SUB)
363375-01	MANUAL, USERS EFIGS
312864-02	CABLE ASSY MINI DIN TO DB25 (QTY=7)
318882-01	CARD WARRANTY CANADA
318928-01	BAG ANTI STATIC
318896-01	S/W LICENSE AGREEMENT
317769-01	DISKETTE ASSY
318940-01	SPACER CARDBOARD
312860-01	PCB ASSY
318733-02	MANUAL AMIGATERM
318556-02	CARD DISK EXCHANGE CANADA

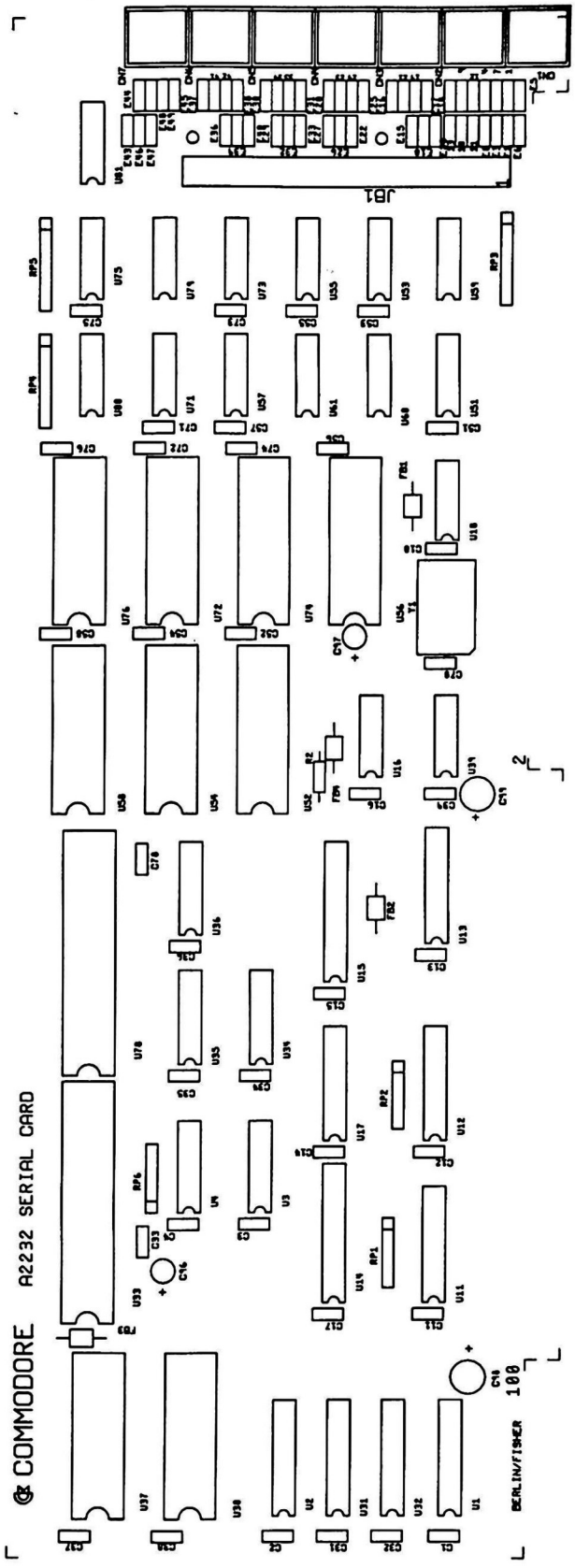
312859-04	A2232 SHIPPING ASSY (AUSTRALIA)
363128-01	BOX PACKING
363127-01	BOX BULK SHIPPING
363100-01	MANUAL, USERS (SUB)
363375-01	MANUAL, USERS EFIGS
312864-02	CABLE ASSY MINI DIN TO DB25 (QTY=7)
318884-01	CARD WARRANTY AUSTRALIA
318928-01	BAG ANTI STATIC
317769-01	DISKETTE ASSY
318940-01	SPACER CARDBOARD
312860-01	PCB ASSY
318733-02	MANUAL AMIGATERM

Commodore International Spare Parts List
PCB Components
PCB Assembly #311611-01

Commodore part numbers are provided for reference only and do not indicate the availability of spare parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Part number information may vary according to country, some parts may not be available in all countries.

IC COMPONENTS		
312860-01	PCB ASSY A2232 SERIAL CARD	
318029-03	8520A-1	U78
390373-01	16R8A PAL	U13
390370-02	16L8 PAL	U17
390371-02	20L8A PAL	U15
390372-03	20L8B PAL	U14
901521-06	74LS74	U18
901522-30	7407	U39
390077-01	74F32	U16
318041-01	74F521	U12
901521-16	74LS138	U36
901521-46	74LS245	U31,U32
390091-01	74F257	U3,U4,U34,U35
901521-29	74LS373	U11
318092-01	74ALS245	U1,U2
901882-01	MC1488 QUAD DRIVER	U59-U61,U79-U81
901883-01	MC1489 QUAD RECEIVER	U51,U53,U55,U57,U71, U73,U75
901895-03	6551A UART	U52,U54,U56,U58,U72, U74,U76
310024-02	8K X 8 SRAM 100 NS	U37,U38
390375-02	LSI CPU 65CE02	U33
901895-02	6551A UART	SUB FOR ITEM 21
SOCKETS		
904150-08	20 PIN DIP	U13,U17
390060-01	24 PIN DIP SOCKET	U14,U15
904150-05	28 PIN DIP	U52,U54,U56,U58,U72, U74,U76
904150-06	40 PIN DIP	U33,U78

RESISTORS		
902441-22	PAK 6 PIN SIP 1K	RP1,RP6
902441-31	PAK 6 PIN SIP 4.7K	RP2
902442-55	PAK 8 PIN SIP 4.7K	RP3-RP5
901550-01	1K 5% ¼ WATT	R2
901550-18	2.2K 5% ¼ WATT	R3,R4
CAPACITORS		
900020-01	.1 UF –50V 20%	C1-C4,C11-C18,C31-C39, C51-C58,C70-C76,C78
390101-05	ELECT ALUM RAD LEAD 4.7 UF	C96-C99
MISCELLANEOUS		
325566-16	OSCILLATOR 1.8432 MHZ	Y1
251842-04	EMI FILTER 470PF	EMI 1-EMI 49
903025-01	FERRITE BEAD	FB1-FB4
903345-29	CONN 56 PIN DIL HEADER .10 CENTERS	JB1
390043-01	SHUNT FEMALE 2 POS	
390218-02	CONN 8 PIN MINI DIN RECEPTACLE	CN1-CN7
312865-01	EXTENSION CARD PANEL	
906800-05	SCREW 3M X 6 LG PAN HEAD PHILLIPS - QTY 2	
316914-01	LABEL FCC ID A2232	

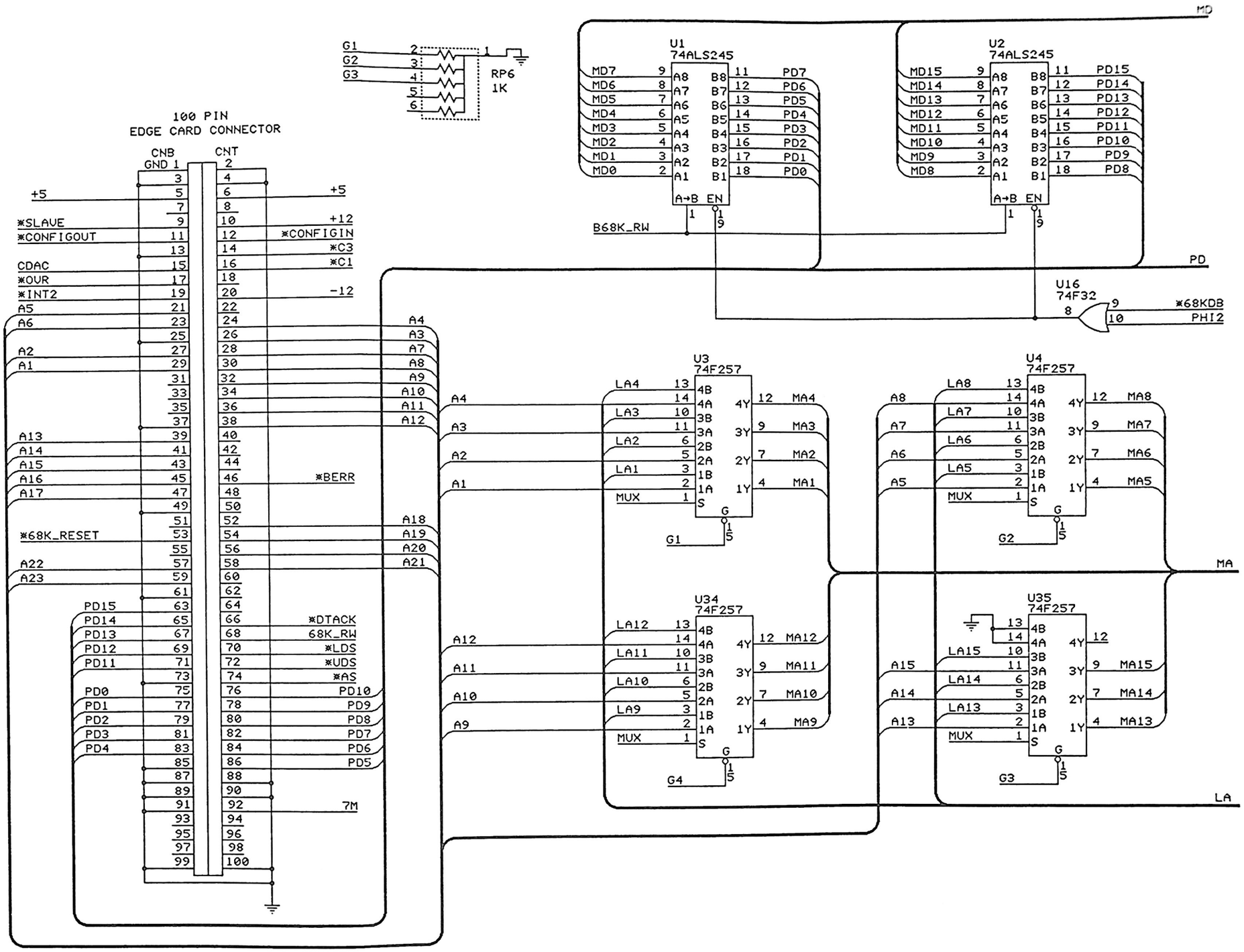


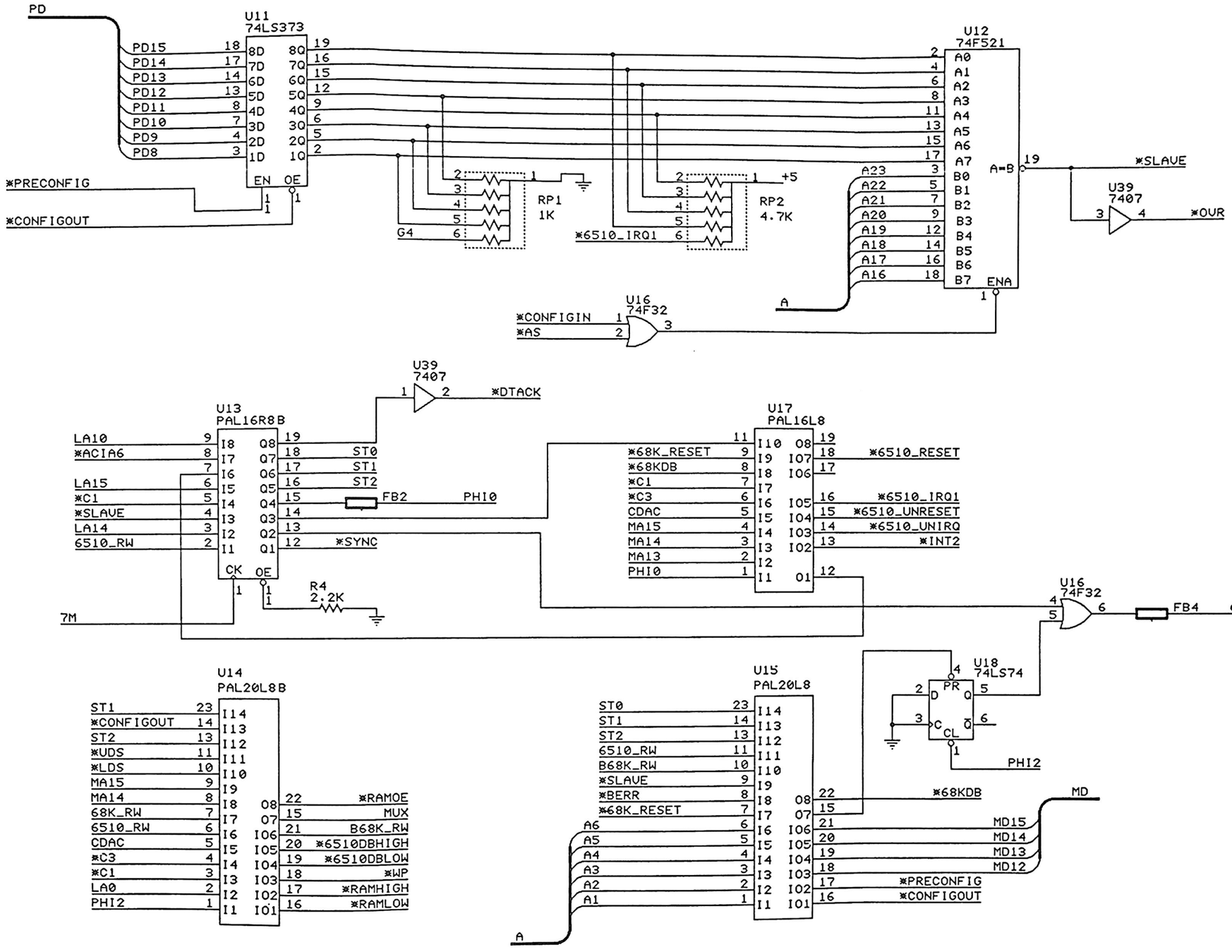
PCB BOARD LAYOUT #312863, REV. 5

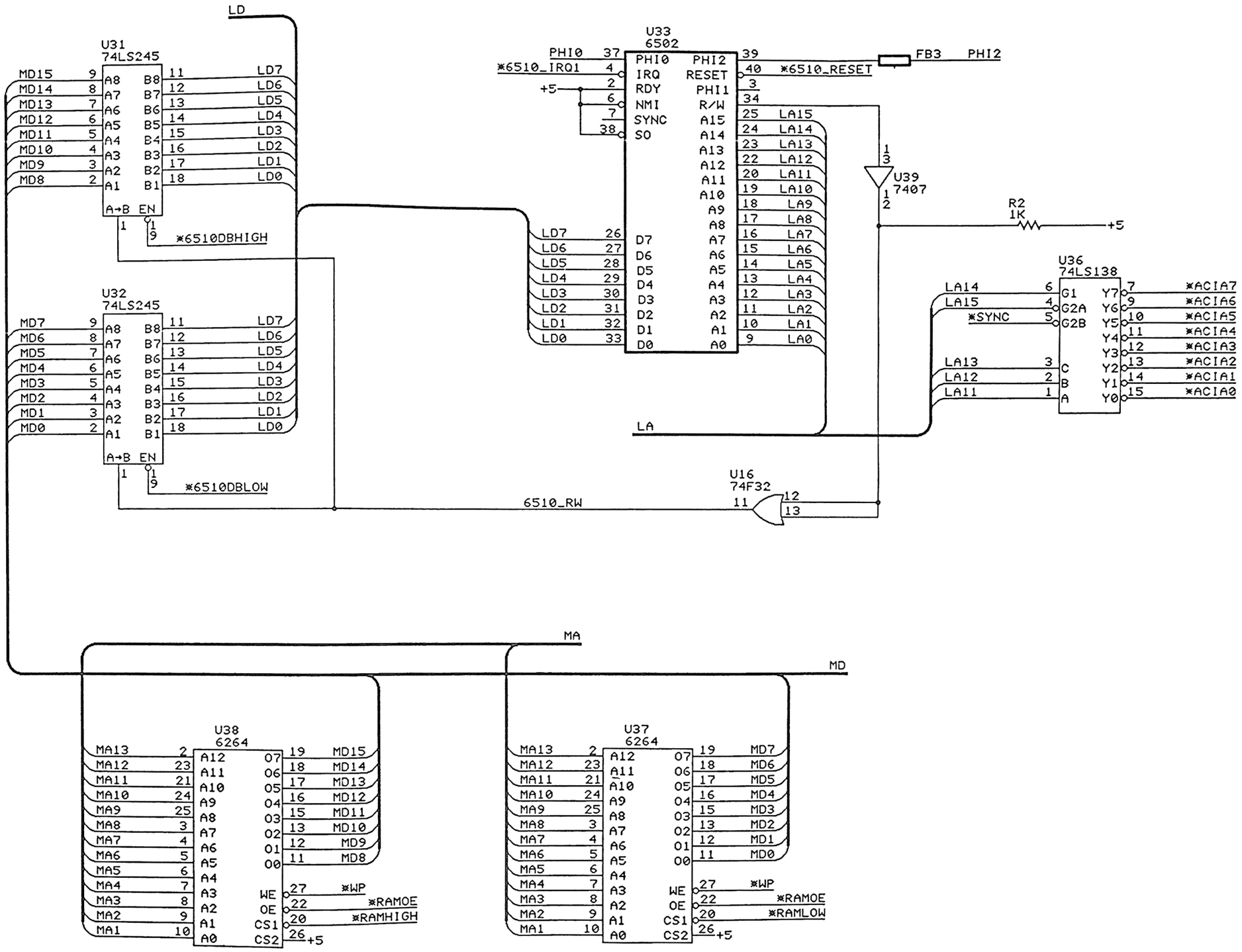
A2232 SCHEMATIC #312861, REV. A — SCHEMATIC PAGE INDEX

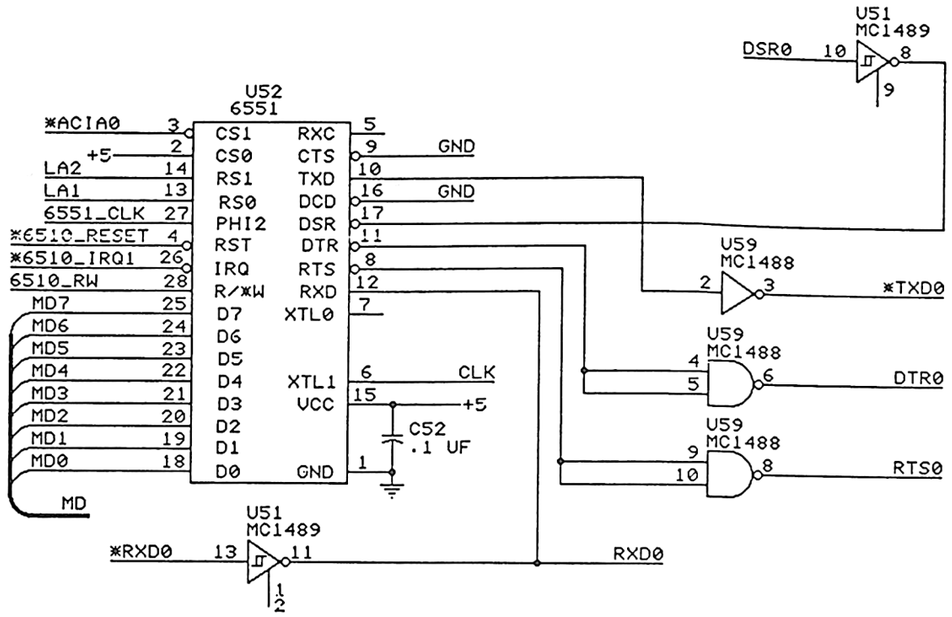
Sheet 1 of 8

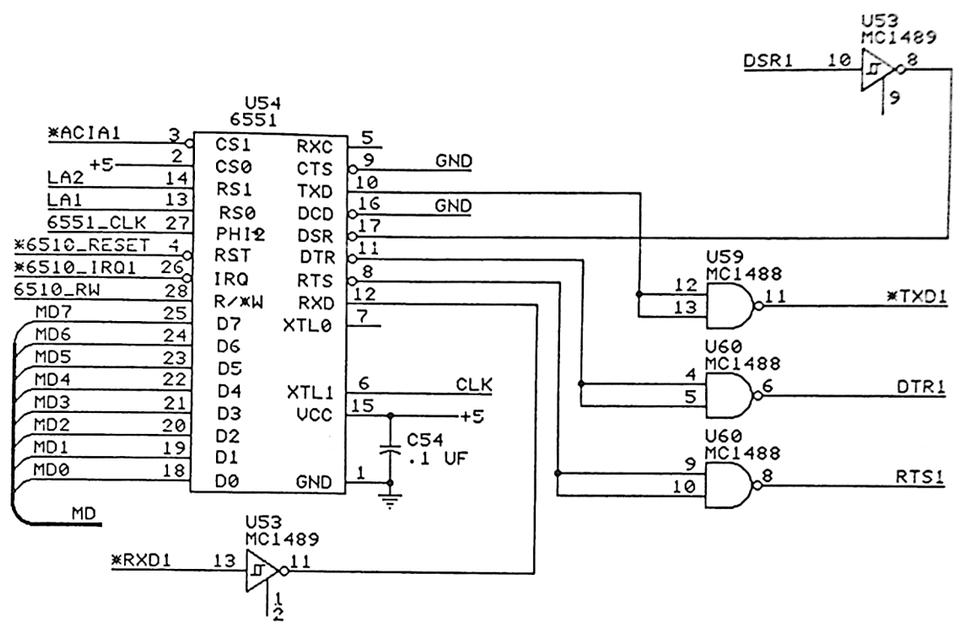
TITLE	SHEET	PAGE
A2232 SCHEMATIC PAGE INDEX	1 of 8	3-15
A2232 SERIAL CARD — EXPANSION BUS CONNECTOR, ADDRESS & DATA BUFFERS	2 of 8	3-16
A2232 SERIAL CARD — AUTOCONFIG STUFF, MISC. CONTROL SIGNALS	3 of 8	3-17
A2232 SERIAL CARD — 6510 INTERFACE, SHARED RAM	4 of 8	3-18
A2232 SERIAL CARD — SERIAL PORTS	5 of 8	3-19
A2232 SERIAL CARD — SERIAL PORTS	6 of 8	3-20
A2232 SERIAL CARD	7 of 8	3-21
A2232 SERIAL CARD — BYPASS CAPS, SPARES	8 of 8	3-22

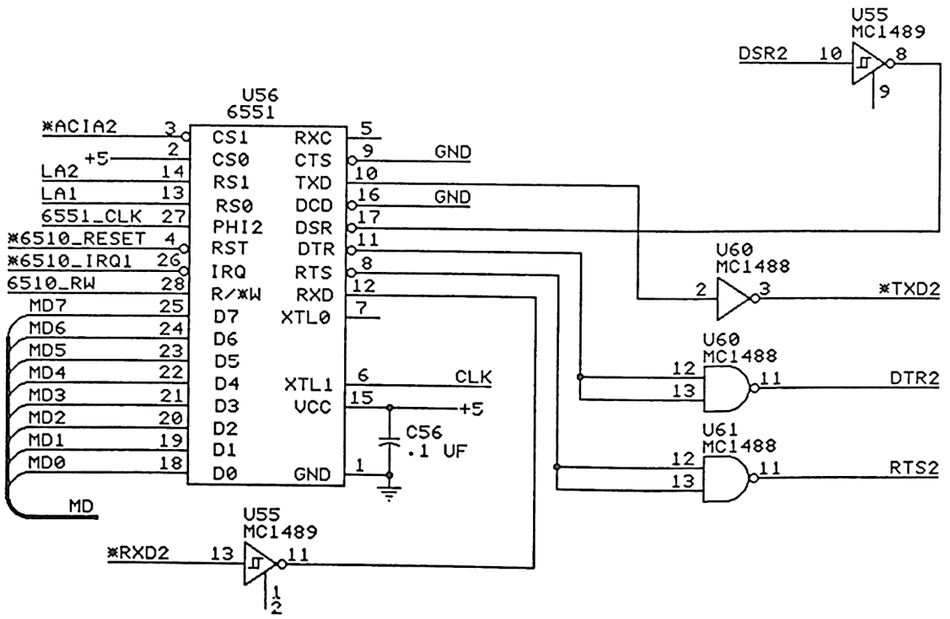

RP6
1K
100 PIN
EDGE CARD CONNECTOR
CNB
CNT
U1
74ALS245
U2
74ALS245
MD
PD
U16
74F32
*68KDB
PHI2
B68K_RW
U3
74F257
U4
74F257
U34
74F257
U35
74F257
MA
LA
*SLAVE
*CONFIGOUT
CDAC
*OUR
*INT2
*68K_RESET
*BERR
*DTACK
68K_RW
*LDS
*UDS
*AS
7M
*CONFIGIN
*C3
*C1
MUX

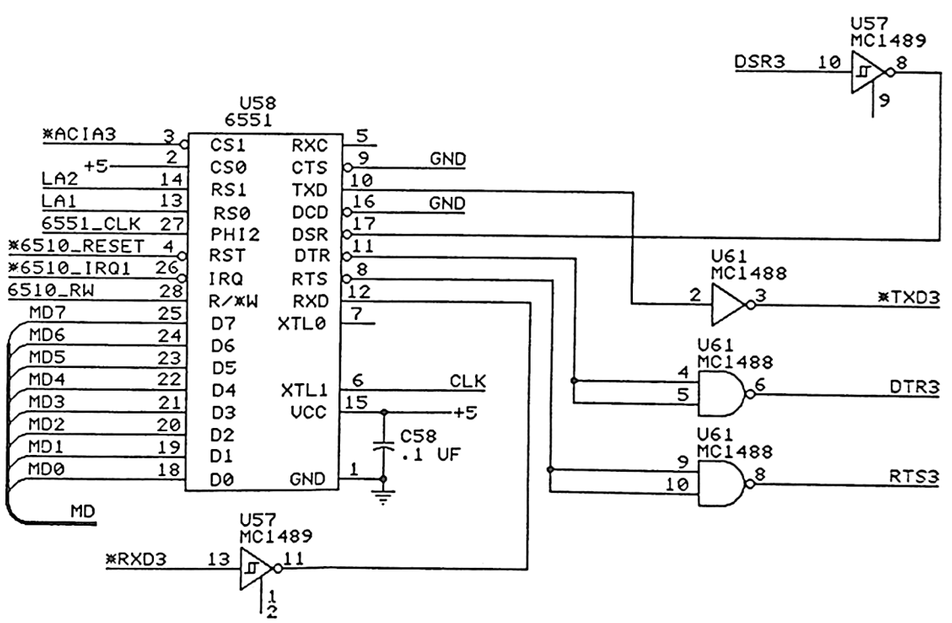

PD
U11
74LS373
PD15
PD14
PD13
PD12
PD11
PD10
PD9
PD8
8D
7D
6D
5D
4D
3D
2D
1D
8Q
7Q
6Q
5Q
4Q
3Q
2Q
1Q
EN
OE
*PRECONFIG
*CONFIGOUT
G4
RP1
1K
*6510_IRQ1
RP2
4.7K
+5
U12
74F521
A0
A1
A2
A3
A4
A5
A6
A7
B0
B1
B2
B3
B4
B5
B6
B7
A=B
ENA
A23
A22
A21
A20
A19
A18
A17
A16
A
U16
74F32
*CONFIGIN
*AS
*SLAVE
U39
7407
*OUR
U39
7407
*DTACK
U13
PAL16R8B
LA10
*ACIA6
LA15
*C1
*SLAVE
LA14
6510_RW
I8
I7
I6
I5
I4
I3
I2
I1
Q8
Q7
Q6
Q5
Q4
Q3
Q2
Q1
CK
OE
ST0
ST1
ST2
FB2
PHI0
*SYNC
R4
2.2K
7M
U17
PAL16L8
*68K_RESET
*68KDB
*C1
*C3
CDAC
MA15
MA14
MA13
PHI0
I10
I9
I8
I7
I6
I5
I4
I3
I2
I1
O8
O7
O6
O5
O4
O3
O2
O1
*6510_RESET
*6510_IRQ1
*6510_UNRESET
*6510_UNIRQ
*INT2
U16
74F32
FB4
6551_CLK
U14
PAL20L8B
ST1
*CONFIGOUT
ST2
*UDS
*LDS
MA15
MA14
68K_RW
6510_RW
CDAC
*C3
*C1
LA0
PHI2
*RAMOE
MUX
B68K_RW
*6510DBHIGH
*6510DBLOW
*WP
*RAMHIGH
*RAMLOW
U15
PAL20L8
ST0
ST1
ST2
6510_RW
B68K_RW
*SLAVE
*BERR
*68K_RESET
A6
A5
A4
A3
A2
A1
A
U18
74LS74
PR
D
C
CL
Q
PHI2
*68KDB
MD
MD15
MD14
MD13
MD12
*PRECONFIG
*CONFIGOUT

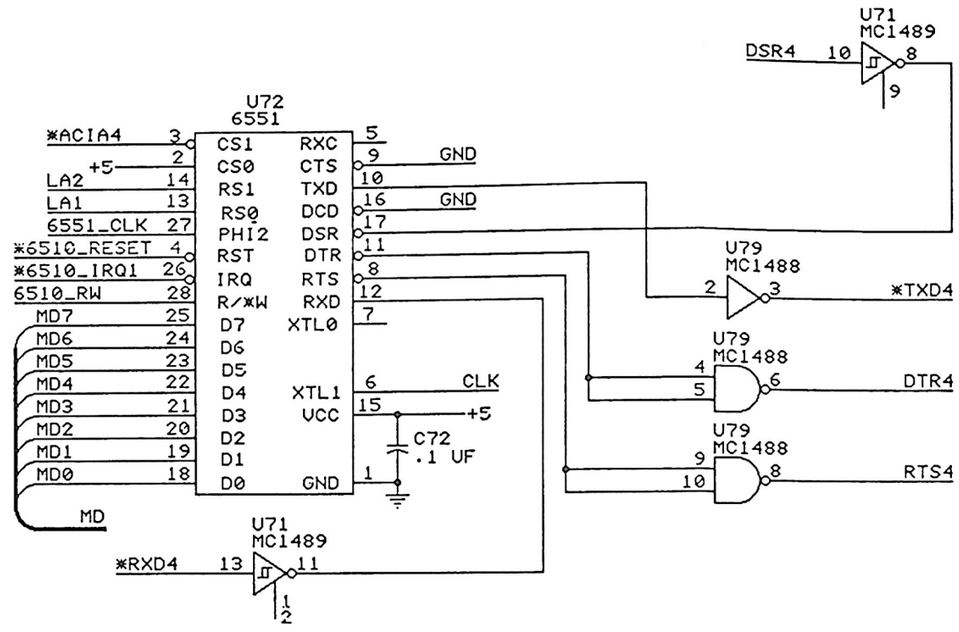

LD
U31
74LS245
MD15 9
MD14 8
MD13 7
MD12 6
MD11 5
MD10 4
MD9 3
MD8 2
A8 A7 A6 A5 A4 A3 A2 A1
B8 B7 B6 B5 B4 B3 B2 B1
11 12 13 14 15 16 17 18
LD7 LD6 LD5 LD4 LD3 LD2 LD1 LD0
A→B EN
1
19
*6510DBHIGH
U32
74LS245
MD7 9
MD6 8
MD5 7
MD4 6
MD3 5
MD2 4
MD1 3
MD0 2
*6510DBLOW
U33
6502
PHI0 37
*6510_IRQ1 4
+5
2
6
7
38
PHI0 IRQ RDY NMI SYNC SO
PHI2 RESET PHI1 R/W
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
39
40
3
34
25 24 23 22 20 19 18 17 16 15 14 13 12 11 10 9
LA15 LA14 LA13 LA12 LA11 LA10 LA9 LA8 LA7 LA6 LA5 LA4 LA3 LA2 LA1 LA0
FB3
PHI2
*6510_RESET
LD7 26
LD6 27
LD5 28
LD4 29
LD3 30
LD2 31
LD1 32
LD0 33
D7 D6 D5 D4 D3 D2 D1 D0
LA
1/3
U39
7407
1/2
R2
1K
+5
U36
74LS138
LA14 6
LA15 4
*SYNC 5
G1 G2A G2B
LA13 3
LA12 2
LA11 1
C B A
Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
7 9 10 11 12 13 14 15
*ACIA7 *ACIA6 *ACIA5 *ACIA4 *ACIA3 *ACIA2 *ACIA1 *ACIA0
U16
74F32
11
12
13
6510_RW
MA
MD
U38
6264
MA13 2
MA12 23
MA11 21
MA10 24
MA9 25
MA8 3
MA7 4
MA6 5
MA5 6
MA4 7
MA3 8
MA2 9
MA1 10
A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
O7 O6 O5 O4 O3 O2 O1 O0
19 18 17 16 15 13 12 11
MD15 MD14 MD13 MD12 MD11 MD10 MD9 MD8
WE OE CS1 CS2
27 22 20 26
*WP *RAMOE *RAMHIGH +5
U37
6264
MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0
*WP *RAMOE *RAMLOW +5

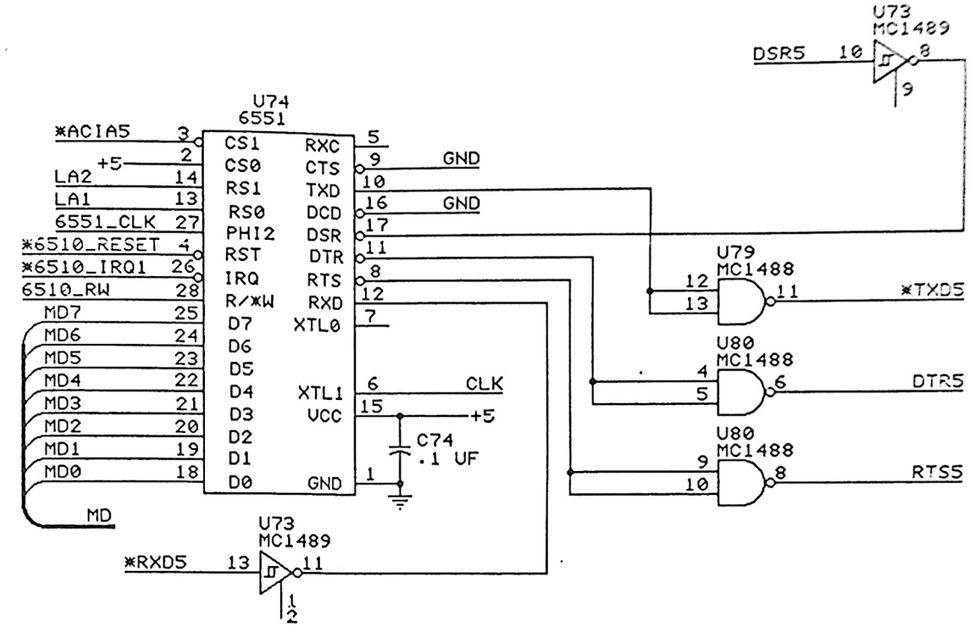

U52
6551
*ACIA0
+5
LA2
LA1
6551_CLK
*6510_RESET
*6510_IRQ1
6510_RW
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
MD
CS1
CS0
RS1
RS0
PHI2
RST
IRQ
R/*W
D7
D6
D5
D4
D3
D2
D1
D0
RXC
CTS
TXD
DCD
DSR
DTR
RTS
RXD
XTL0
XTL1
VCC
GND
GND
GND
CLK
+5
C52
.1 UF
U51
MC1489
DSR0
*RXD0
RXD0
U59
MC1488
*TXD0
DTR0
RTS0

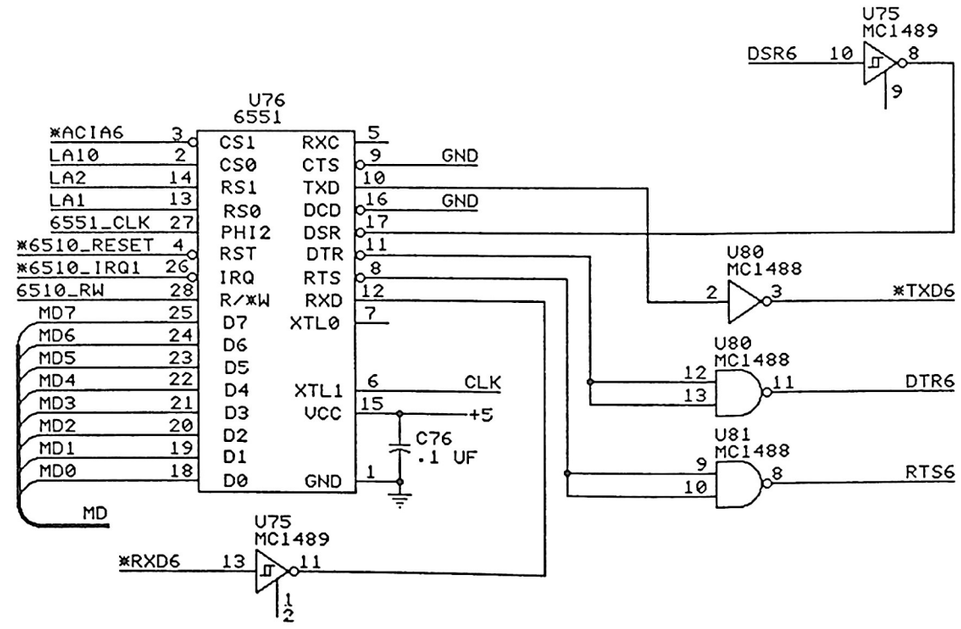

U54
6551
*ACIA1
+5
LA2
LA1
6551_CLK
*6510_RESET
*6510_IRQ1
6510_RW
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
MD
CS1
CS0
RS1
RS0
PHI2
RST
IRQ
R/*W
D7
D6
D5
D4
D3
D2
D1
D0
RXC
CTS
TXD
DCD
DSR
DTR
RTS
RXD
XTL0
XTL1
VCC
GND
GND
GND
CLK
+5
C54
.1 UF
U53
MC1489
DSR1
*RXD1
U59
MC1488
U60
MC1488
*TXD1
DTR1
RTS1

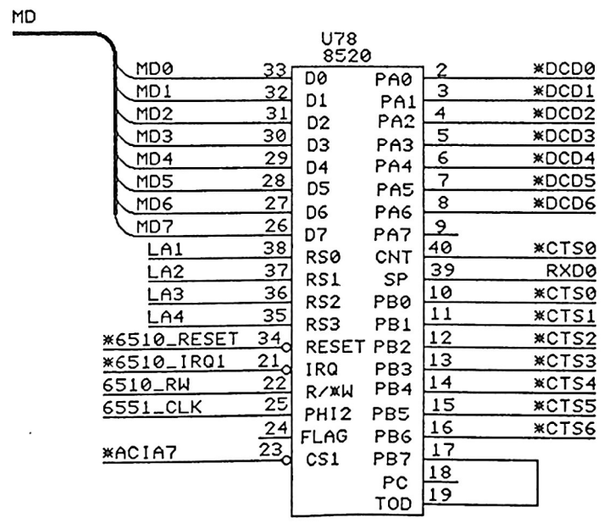

U56
6551
*ACIA2
+5
LA2
LA1
6551_CLK
*6510_RESET
*6510_IRQ1
6510_RW
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
MD
CS1
CS0
RS1
RS0
PHI2
RST
IRQ
R/*W
D7
D6
D5
D4
D3
D2
D1
D0
RXC
CTS
TXD
DCD
DSR
DTR
RTS
RXD
XTL0
XTL1
VCC
GND
GND
GND
CLK
+5
C56
.1 UF
U55
MC1489
DSR2
*RXD2
U60
MC1488
*TXD2
DTR2
RTS2

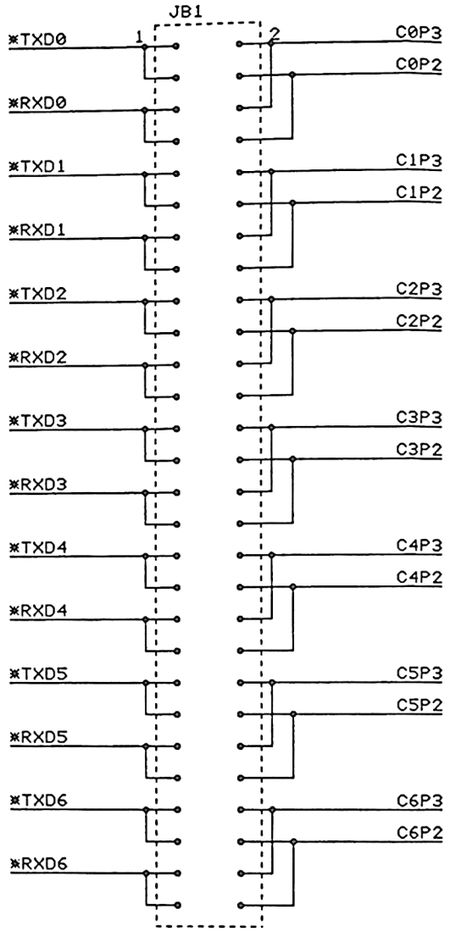

U58
6551
*ACIA3
+5
LA2
LA1
6551_CLK
*6510_RESET
*6510_IRQ1
6510_RW
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
MD
CS1
CS0
RS1
RS0
PHI2
RST
IRQ
R/*W
D7
D6
D5
D4
D3
D2
D1
D0
RXC
CTS
TXD
DCD
DSR
DTR
RTS
RXD
XTL0
XTL1
VCC
GND
GND
GND
CLK
+5
C58
.1 UF
U57
MC1489
DSR3
*RXD3
U61
MC1488
*TXD3
DTR3
RTS3

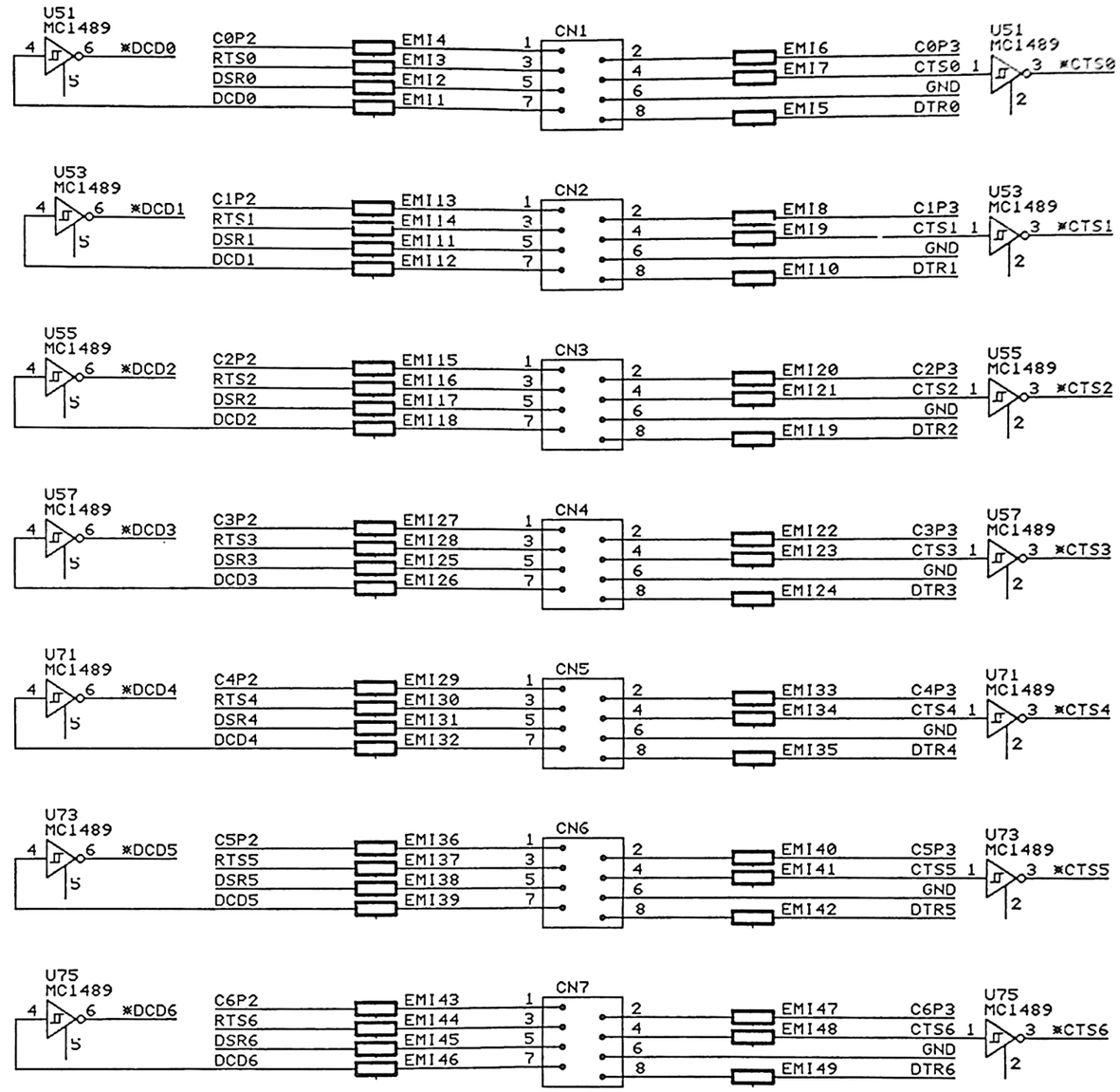

U72
6551
*ACIA4
+5
LA2
LA1
6551_CLK
*6510_RESET
*6510_IRQ1
6510_RW
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
MD
CS1
CS0
RS1
RS0
PHI2
RST
IRQ
R/*W
D7
D6
D5
D4
D3
D2
D1
D0
RXC
CTS
TXD
DCD
DSR
DTR
RTS
RXD
XTL0
XTL1
VCC
GND
GND
GND
CLK
+5
C72
.1 UF
U71
MC1489
DSR4
U79
MC1488
*TXD4
U79
MC1488
DTR4
U79
MC1488
RTS4
U71
MC1489
*RXD4


U74
6551
*ACIA5
+5
LA2
LA1
6551_CLK
*6510_RESET
*6510_IRQ1
6510_RW
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
MD
CS1
CS0
RS1
RS0
PHI2
RST
IRQ
R/*W
D7
D6
D5
D4
D3
D2
D1
D0
RXC
CTS
TXD
DCD
DSR
DTR
RTS
RXD
XTL0
XTL1
VCC
GND
GND
GND
CLK
+5
C74
.1 UF
U73
MC1489
DSR5
U79
MC1488
*TXD5
U80
MC1488
DTR5
U80
MC1488
RTS5
U73
MC1489
*RXD5


U76
6551
*ACIA6
LA10
LA2
LA1
6551_CLK
*6510_RESET
*6510_IRQ1
6510_RW
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
MD
CS1
CS0
RS1
RS0
PHI2
RST
IRQ
R/*W
D7
D6
D5
D4
D3
D2
D1
D0
RXC
CTS
TXD
DCD
DSR
DTR
RTS
RXD
XTL0
XTL1
VCC
GND
GND
GND
CLK
+5
C76
.1 UF
U75
MC1489
DSR6
U80
MC1488
*TXD6
U80
MC1488
DTR6
U81
MC1488
RTS6
U75
MC1489
*RXD6


MD
U78
8520
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
LA1
LA2
LA3
LA4
*6510_RESET
*6510_IRQ1
6510_RW
6551_CLK
*ACIA7
D0
D1
D2
D3
D4
D5
D6
D7
RS0
RS1
RS2
RS3
RESET
IRQ
R/*W
PHI2
FLAG
CS1
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
CNT
SP
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC
TOD
*DCD0
*DCD1
*DCD2
*DCD3
*DCD4
*DCD5
*DCD6
*CTS0
RXD0
*CTS0
*CTS1
*CTS2
*CTS3
*CTS4
*CTS5
*CTS6


JB1
*TXD0
*RXD0
*TXD1
*RXD1
*TXD2
*RXD2
*TXD3
*RXD3
*TXD4
*RXD4
*TXD5
*RXD5
*TXD6
*RXD6
C0P3
C0P2
C1P3
C1P2
C2P3
C2P2
C3P3
C3P2
C4P3
C4P2
C5P3
C5P2
C6P3
C6P2


U51
MC1489
*DCD0
C0P2
RTS0
DSR0
DCD0
CN1
EMI4
EMI3
EMI2
EMI1
EMI6
EMI7
EMI5
C0P3
CTS0
GND
DTR0
*CTS0
U53
MC1489
*DCD1
C1P2
RTS1
DSR1
DCD1
CN2
EMI13
EMI14
EMI11
EMI12
EMI8
EMI9
EMI10
C1P3
CTS1
GND
DTR1
*CTS1
U55
MC1489
*DCD2
C2P2
RTS2
DSR2
DCD2
CN3
EMI15
EMI16
EMI17
EMI18
EMI20
EMI21
EMI19
C2P3
CTS2
GND
DTR2
*CTS2
U57
MC1489
*DCD3
C3P2
RTS3
DSR3
DCD3
CN4
EMI27
EMI28
EMI25
EMI26
EMI22
EMI23
EMI24
C3P3
CTS3
GND
DTR3
*CTS3
U71
MC1489
*DCD4
C4P2
RTS4
DSR4
DCD4
CN5
EMI29
EMI30
EMI31
EMI32
EMI33
EMI34
EMI35
C4P3
CTS4
GND
DTR4
*CTS4
U73
MC1489
*DCD5
C5P2
RTS5
DSR5
DCD5
CN6
EMI36
EMI37
EMI38
EMI39
EMI40
EMI41
EMI42
C5P3
CTS5
GND
DTR5
*CTS5
U75
MC1489
*DCD6
C6P2
RTS6
DSR6
DCD6
CN7
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GND
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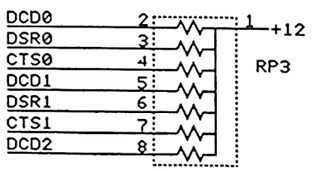
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CTS1
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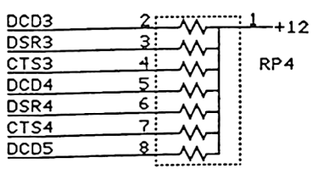
+12
RP3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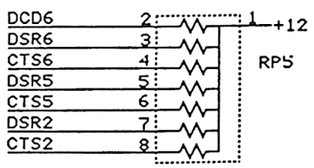
DSR3
CTS3
DCD4
DSR4
CTS4
DCD5
+12
RP4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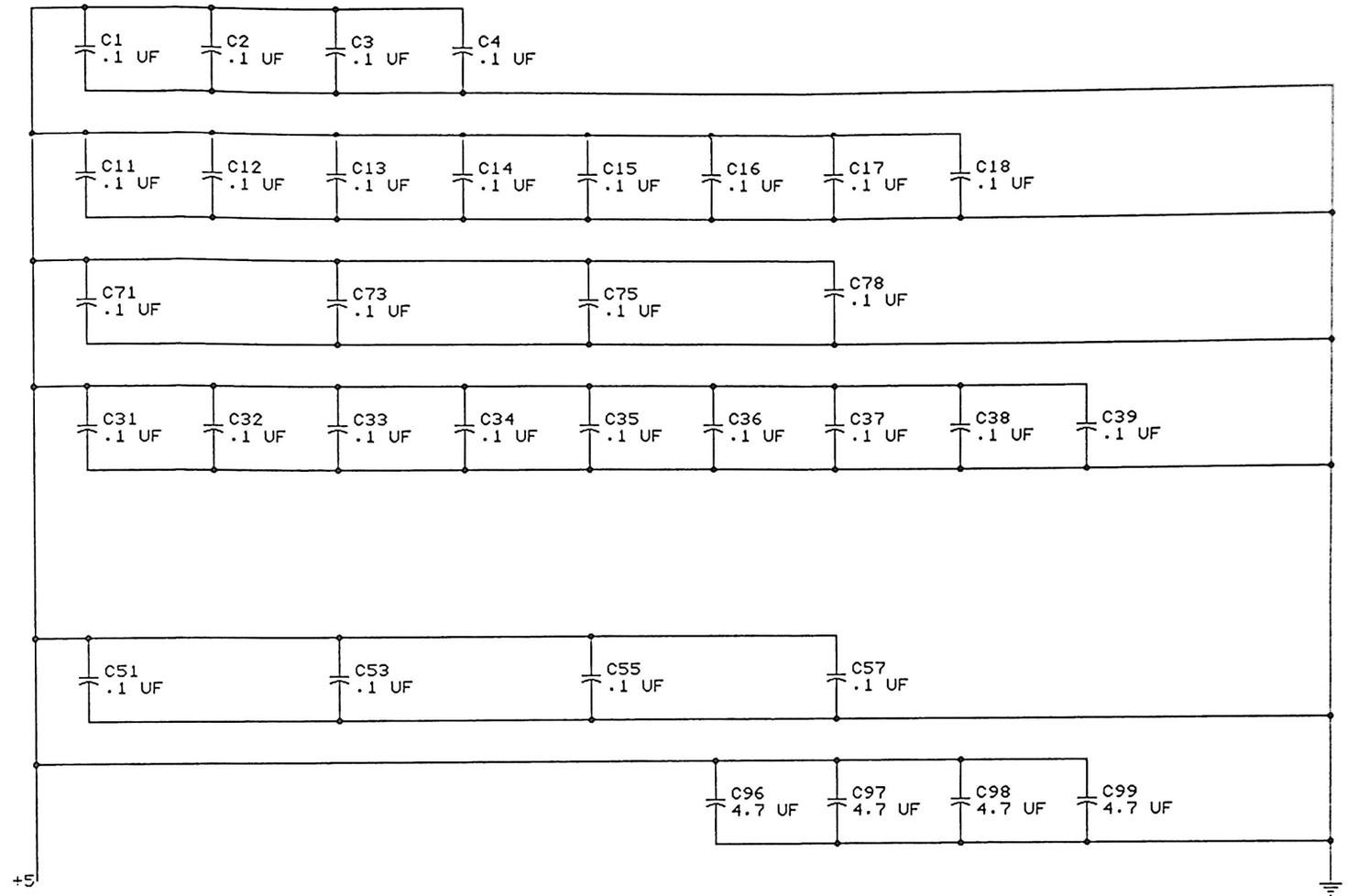
CTS6
DSR5
CTS5
DSR2
CTS2
+12
RP5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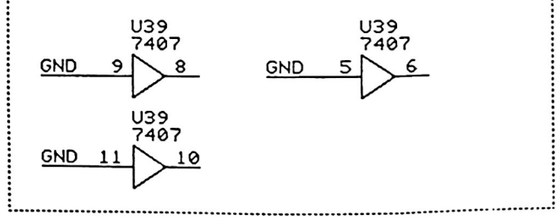
C2 .1 UF
C3 .1 UF
C4 .1 UF
C11 .1 UF
C12 .1 UF
C13 .1 UF
C14 .1 UF
C15 .1 UF
C16 .1 UF
C17 .1 UF
C18 .1 UF
C71 .1 UF
C73 .1 UF
C75 .1 UF
C78 .1 UF
C31 .1 UF
C32 .1 UF
C33 .1 UF
C34 .1 UF
C35 .1 UF
C36 .1 UF
C37 .1 UF
C38 .1 UF
C39 .1 UF
C51 .1 UF
C53 .1 UF
C55 .1 UF
C57 .1 UF
C96 4.7 UF
C97 4.7 UF
C98 4.7 UF
C99 4.7 UF
+5

SPARES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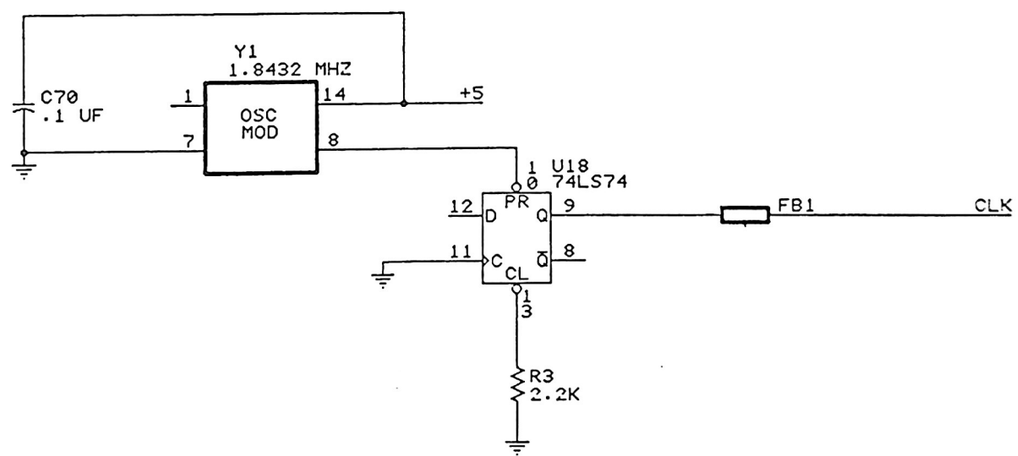
GND 9 8
U39 7407
GND 5 6
U39 7407
GND 11 10


Y1 1.8432 MHZ
C70 .1 UF
1
7
OSC MOD
14
8
+5
1 U18 0 74LS74
12 D
PR
Q 9
FB1
CLK
11 C
CL
Q 8
1 3
R3 2.2K

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